

RELIABILITY REPORT

FOR

MAX3803UBP

Chip Scale Devices

December 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3803 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3803 equalizer automatically provides compensation for transmission-medium losses encountered with FR4 stripline and cable in an incredibly small 2mm x 2.5mm package. It is ideal for backplane applications requiring up to 40in between the line card and the switch card or up to 10m of twin ax cable between racks. Its small size provides placement and routing flexibility. The CML inputs and outputs are DC-coupled and can be terminated to a supply as low as +1.1V. The MAX3803 operates from 0°C to +85°C and consumes 160mW at +3.3V

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage, VCC, VTI, and VTO	-0.5V to +6V
Continuous Output Current	-25mA to +25mA
IN±, OUT±, EN	-0.5V to (VCC + 0.5V)
Operating Ambient Temperature Range	0°C to +85°C
Storage Ambient Temperature Range	-55°C to +150°C

II. Manufacturing Information

A. Description/Function:	DC-Coupled, UCSP 3.125Gbps Equalizer
B. Process:	GST4-F60
C. Number of Device Transistors:	1155
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	December, 2002

III. Packaging Information

A. Package Type:	5 x 4 UCSP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0080
H. Flammability Rating:	Class: UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	103 x 82 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.78 \times 10^{-8} \quad \lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7089) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M & RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HT25 die type has been found to have all pins able to withstand a transient pulse of +/-200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3803UBP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

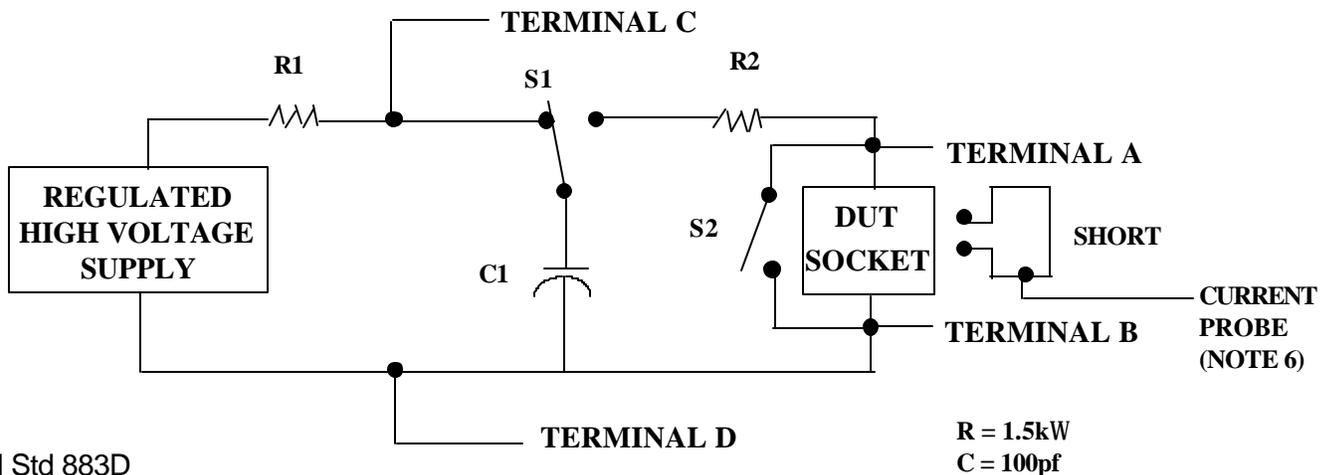
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

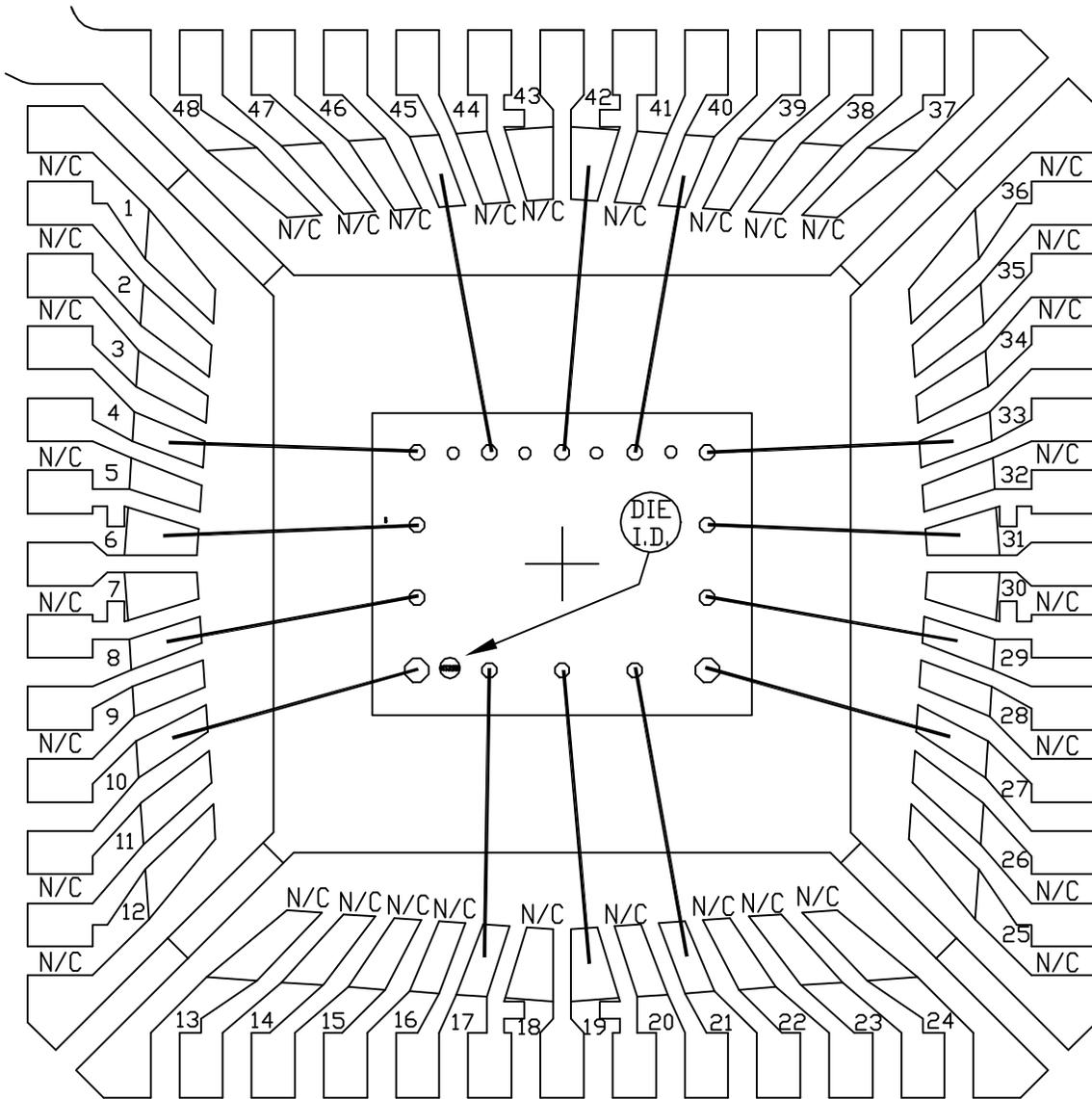
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



EXPOSED PAD PKG.

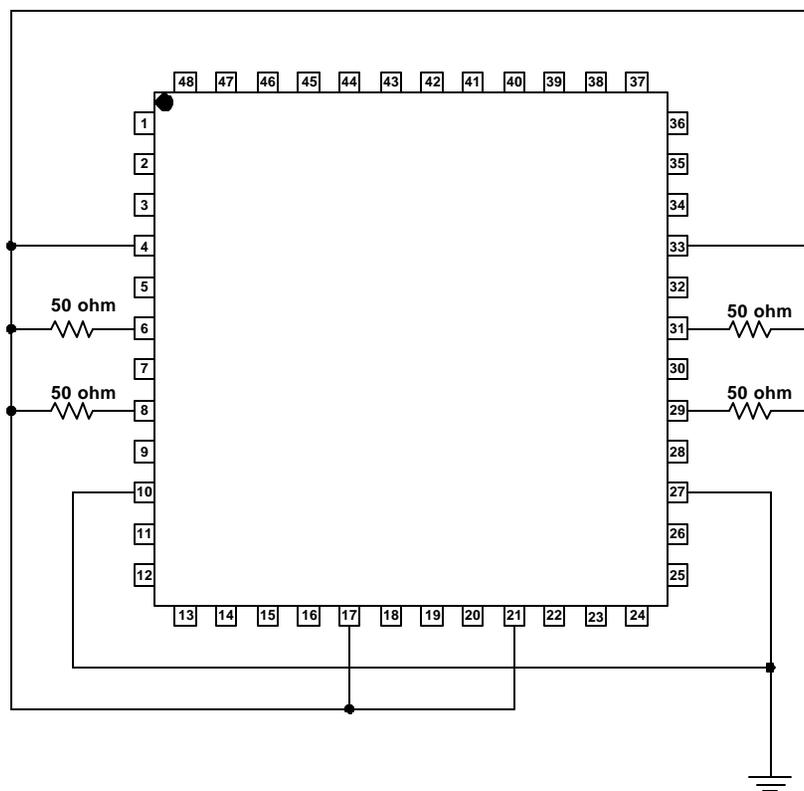


FOR ENGINEERING BUILD ONLY

PKG. CODE: C48E-7		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 157x157	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0080	REV: A

ONCE PER SOCKET

ONCE PER BOARD



+3.6V

DEVICES: MAX 3803
PACKAGE: 48 - TQFP
MAX. EXPECTED CURRENT = 75mA

DRAWN BY: HAK TAN

NOTES: