

RELIABILITY REPORT  
FOR  
**MAX4071AxA**  
PLASTIC ENCAPSULATED DEVICES

January 30, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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## Conclusion

The MAX4071 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

### I. Device Description

#### A. General

The MAX4071 low-cost, bidirectional, high-side, current-sense amplifier is ideal for monitoring battery charge and discharge currents in notebooks, cell phones, and other portable equipment. It features up to 24V input common-mode voltage range, low 100 $\mu$ A supply current (which drops to only 10 $\mu$ A in shutdown), and a total output error of less than 1.5%. The wide 1.35V to 24V input common-mode range is independent of the supply voltage, ensuring that the current-sense feedback remains accurate even when connected to a battery pack in deep discharge.

To achieve maximum flexibility, an external current-sense resistor is used along with a Gain Select pin to choose either 50V/V or 100V/V. A single output pin continuously monitors the transition from charge to discharge and avoids the need for a separate polarity output. The MAX4071 contains an internal 1.5V reference. The charging current is represented by an output voltage from 2.5V to  $V_{CC}$ , while discharge current is given from 2.5V to GND.

The MAX4071 operates from a 2.7V to 24V single supply and the device is specified over the automotive operating temperature range, -40°C to +125°C. The MAX4071 is available in a 8-pin  $\mu$ MAX and 8-pin QFN packages.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC, RS+, RS- to GND	-0.3V to +26V
OUT to GND	-0.3V to Lesser of (VCC + 0.3V) or 15V
Differential Input Voltage (VRS+ - VRS-)	$\pm$ 0.3V
GSEL, SHDN, REFOUT, REFIN and ADJ to GND	-0.3V to (VCC + 0.3V)
OUT Short-Circuit Duration to GND or to Lesser of (VCC or 15V)	Continuous
REFOUT Short Circuit to VCC or GND	Continuous
Current into Any Pin	$\pm$ 20mA
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin $\mu$ Max	362mW
8-Pin QFN	379mW
Derates above +70°C	
8-Pin $\mu$ MAX	4.5mW/°C
8-Pin QFN	4.7mW/°C

## II. Manufacturing Information

A. Description/Function:	Bidirectional, High-Side, Current-Sense Amplifiers with Reference
B. Process:	S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	338
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Malaysia, Thailand or USA
F. Date of Initial Production:	April, 2002

## III. Packaging Information

A. Package Type:	<b>8-Lead uMAX</b>	<b>8-Lead QFN (3x3)</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-2501-0206	# 05-2501-0207
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	59 x 67 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 44 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.68 \times 10^{-9} \quad \lambda = 24.68 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec. # 06-5917) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The OX97 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 50\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4071AxA**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		44	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	uMAX	77	0
			QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Shrink Small Outline package.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

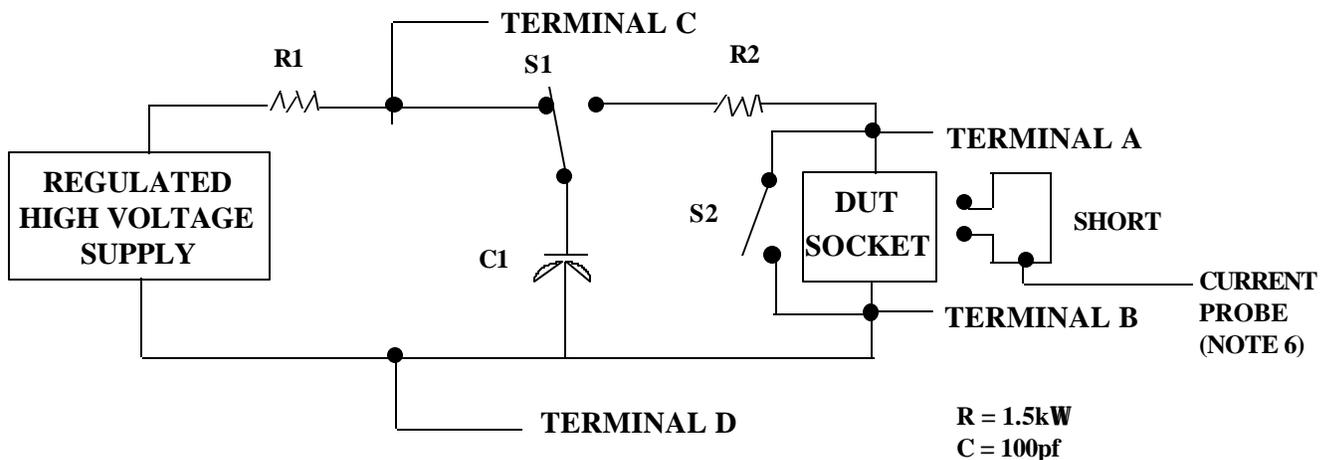
1/ Table II is restated in narrative form in 3.4 below.

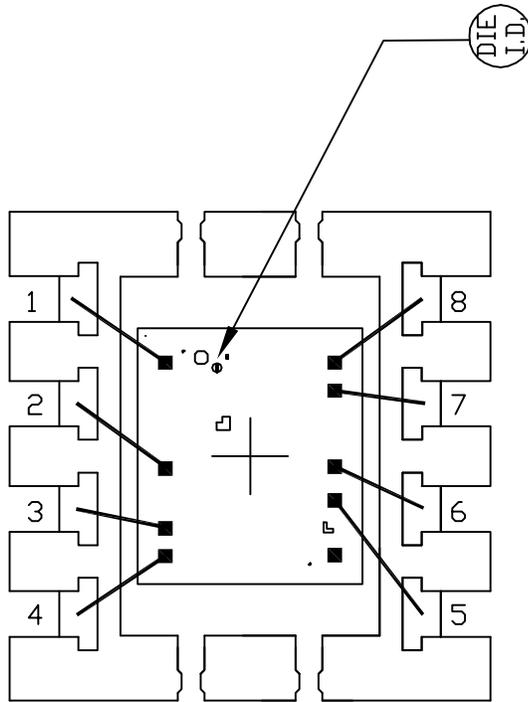
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ ,  $GND$ ,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

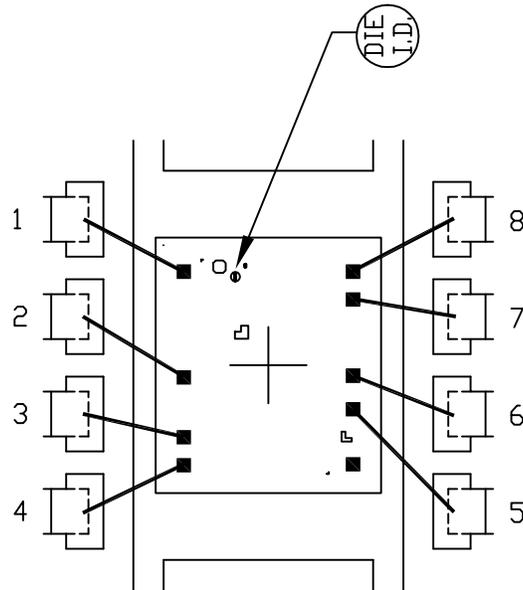




PKG. CODE: U8-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG. DESIGN			BOND DIAGRAM #: 05-2501-0206	REV: A

3x3x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



PKG. CODE: T833-1

SIGNATURES

DATE

**MAXIM**  
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CAV./PAD SIZE:  
71x102

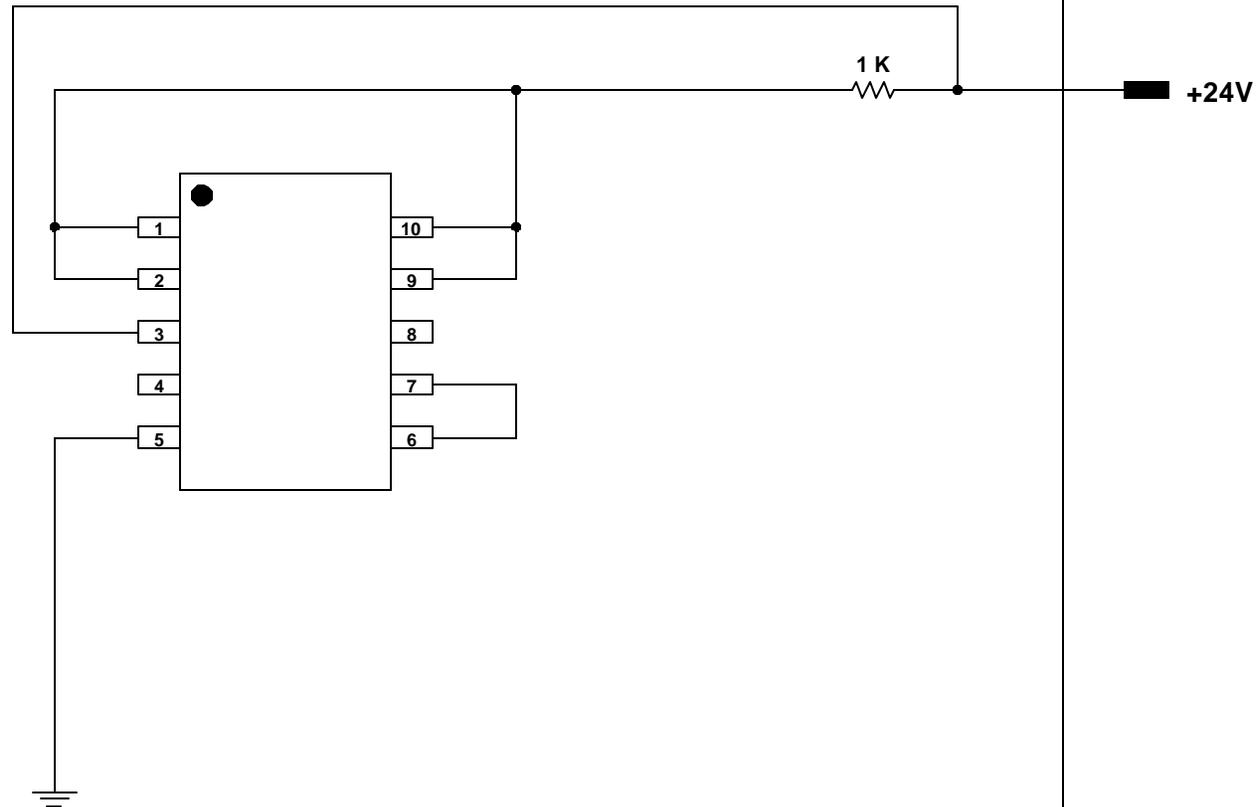
PKG.  
DESIGN

BOND DIAGRAM #:  
05-2501-0207

REV:  
B

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4069EUB (OX97Z)  
PACKAGE: 10-uMAX  
MAX. EXPECTED CURRENT = 0.25 mA

DRAWN BY: TEK TAN  
NOTES: