RELIABILITY REPORT

FOR

MAX4090ExT/AAxT

PLASTIC ENCAPSULATED DEVICES

August 16, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX4090/A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4090 3V/5V, 6dB video buffer with sync-tip clamp, and low-power shutdown mode is available in tiny SOT23 and SC70 packages. The MAX4090 is designed to drive DC-coupled, 150Ω back-terminated video loads in portable video applications such as digital still cams, portable DVD players, digital camcorders, PDAs, video-enabled cell phones, portable game systems, and notebook computers. The input clamp positions the video waveform at the output and allows the MAX4090 to be used as a DC-coupled output driver.

The MAX4090 operates from a single 2.7V to 5.5V supply and consumes only 6.5mA of supply current. The low-power shutdown mode reduces the supply current to 150nA, making the MAX4090 ideal for low-voltage, battery-powered video applications.

The MAX4090 is available in tiny 6-pin SOT23 and SC70 packages and is specified over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6V
OUT, FB, SHDN to GND	-0.3V to (VCC + 0.3V)
IN to GND (Note 1)	VCLP to (VCC + 0.3V)
IN Short-Circuit Duration from -0.3V to VCLP	1min
Output Short-Circuit Duration to VCC or GND	Continuous
Operating Temperature Range	-40°C to +85°C
Operating Temperature Range	
MAX4090E	-40°C to +85°C
MAX4090A	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	695mW
6-Pin SC70	245mW
6-Pin µDFN	290mW
Derates above +70°C	
6-Pin SOT23	8.7mW/°C
6-Pin SC70	3.1mW/°C
6-Pin µDFN	3.6mW/°C

Note 1: VCLP is the input clamp voltage as defined in the *DC Electrical Characteristics* table.

II. Manufacturing Information

A. Description/Function:	3V/5V, 6dB Video Buffer with Sync-Tip Clamp and 150nA Shutdown Current
B. Process:	B6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	755
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	April, 2003

III. Packaging Information

A. Package Type:	**6-Pin SC70**	**6-Pin SOT23**	**6-PIn µDFN**
B. Lead Frame:	Alloy 42	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin		Gold
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0401	#05-9000-0400	#05-9000-0400
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.91 \times 10^{-9}$

λ = 22.91 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6193) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**). Current monitor data for the B6/S6 Process results in a FIT Rate of 0.28 @ 25C and 4.88 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The VA18 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4090ExT/AAxT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70 SOT23 µDFN	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

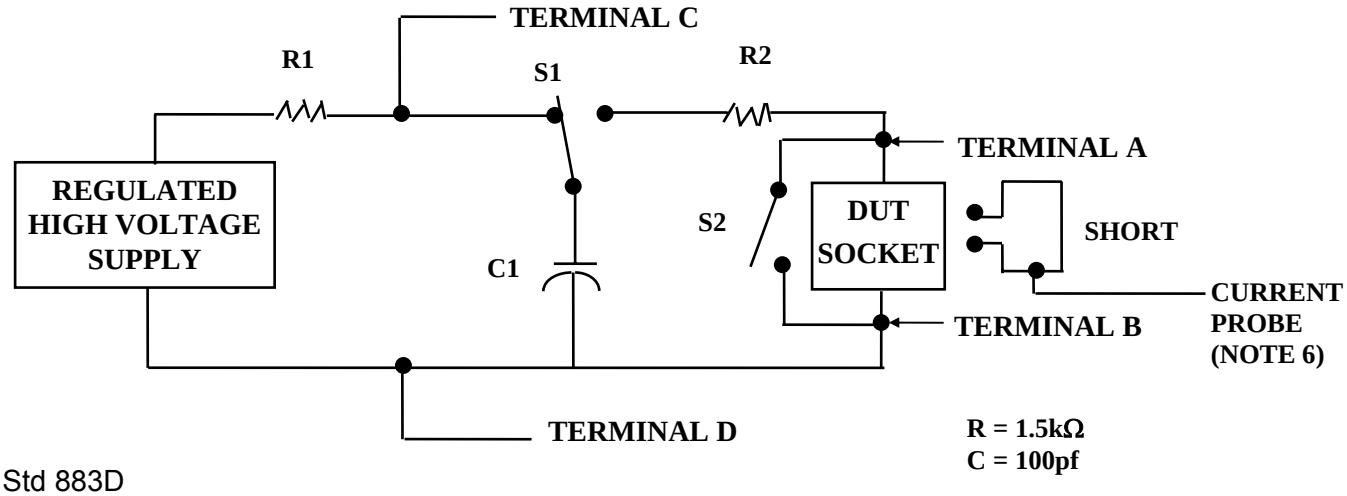
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

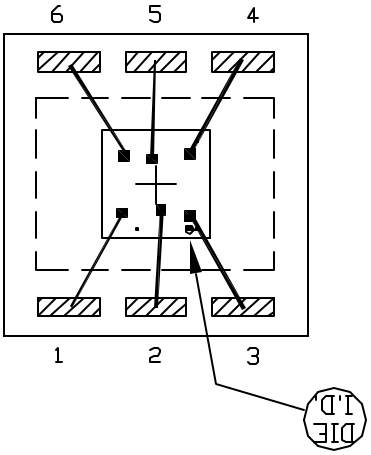
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

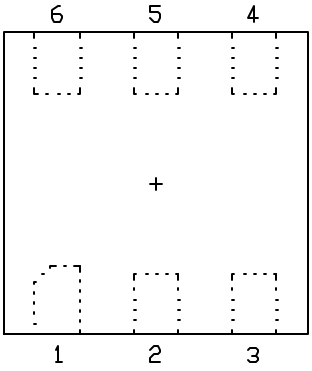


2x2x0.8mm uDFN

TOP VIEW



TOP VIEW OF BOTTOM LEADS

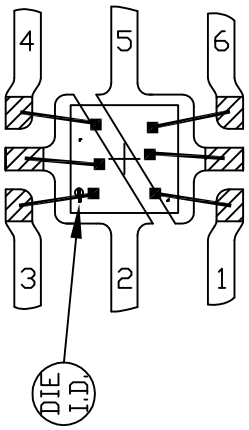


BONDABLE AREA

MAX. DIE PLACEMENT AREA

USE NON-CONDUCTIVE EPOXY

PKG. CODE: L622-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: – –	PKG.			BOND DIAGRAM #: 05-9000-1723	REV: B
	DESIGN				

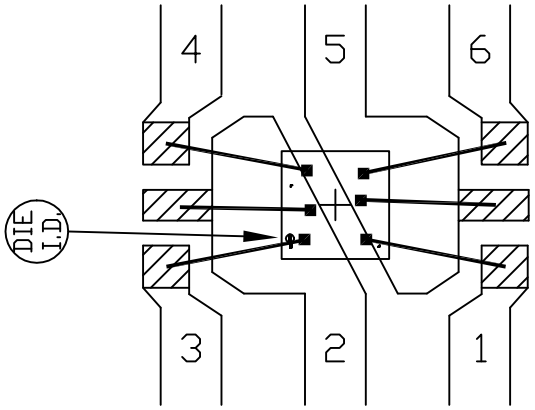


USE NON-CONDUCTIVE EPOXY

NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: X6S-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 36x34	PKG.			BOND DIAGRAM #: 05-9000-0401	REV: A
	DESIGN				



NOTE: USE NON-CONDUCTIVE EPOXY ONLY

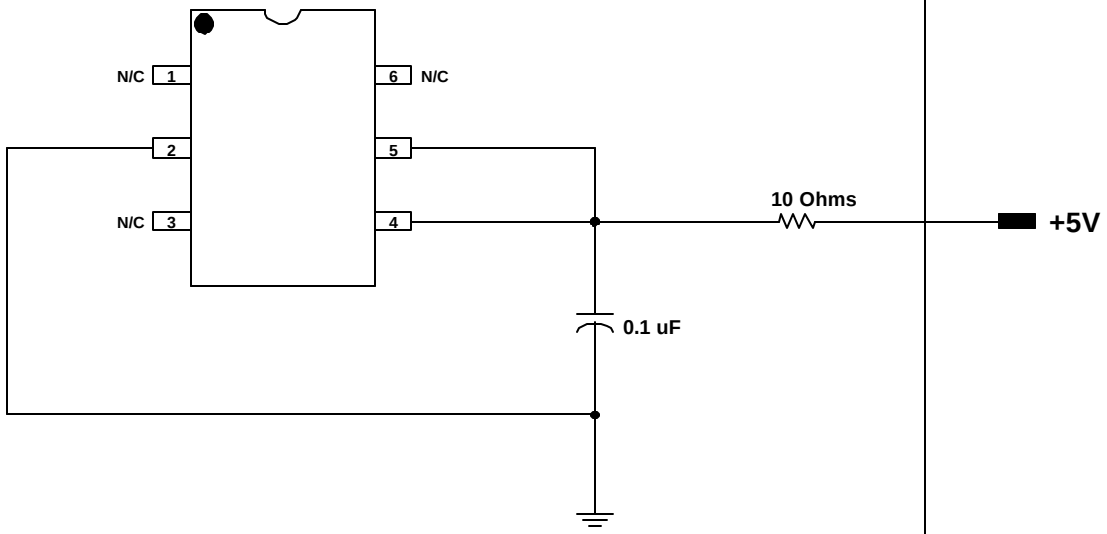
CAVITY DOWN

BONDABLE AREA

PKG. CODE: U6S-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x46	PKG.			BOND DIAGRAM #: 05-9000-0400	REV: A
	DESIGN		10/10/02		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4090 (VA18Z)
PACKAGE: 6-SOT23
MAX. EXPECTED CURRENT = 15mA

NOTES: