RELIABILITY REPORT

FOR

MAX4162ESA+T

PLASTIC ENCAPSULATED DEVICES

February 4, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX4162ESA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX4162/MAX4163/MAX4164 are single/dual/quad, micropower operational amplifiers that combine an exceptional bandwidth to power consumption ratio with true rail-to-rail inputs and outputs. They consume a mere 25µA quiescent current per amplifier, yet achieve 200kHz gain-bandwidth product and are unity-gain stable while driving any capacitive load. The MAX4162/MAX4163/MAX4164 operate from either a single supply (2.5V to 10V) or dual supplies (±1.25V to ±5V), with an input common-mode voltage range that extends 250mV beyond either supply rail. These amplifiers use a proprietary architecture to achieve a very high input common-mode rejection ratio without the midswing nonlinearities present in other rail-to-rail op amps. This architecture also maintains high open-loop gain and output swing while driving substantial loads. The combination of excellent bandwidth/power performance, single-supply operation, and miniature footprint makes these op amps ideal for portable equipment and other low-power, single-supply applications. The single MAX4162 is available in 8-pin SO and space-saving 5-pin SOT23 packages. The MAX4163 is available in an 8-pin ultra chip-scale package (UCSP(tm)) and an 8-pin µMAX® or SO package. The MAX4164 is available in a 14-pin SO package.

II. Manufacturing Information

A. Description/Function:	SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	April 26, 1997

III. Packaging Information

A. Package Type:	8-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3001-0005
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	170°C/W
K. Single Layer Theta Jc:	40°C/W
L. Multi Layer Theta Ja:	136°C/W
M. Multi Layer Theta Jc:	38°C/W

IV. Die Information

A. Dimensions:	38X57 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.03 @ 25C and 0.51 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot BPUAAB003B D/C 9646, Latch-up lot NPUACS001D D/C 9749)

The OP01 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4162ESA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	BPUAAB003D, D/C 9721

Note 1: Life Test Data may represent plastic DIP qualification lots.