MAX4173HExx
Rev. A

RELIABILITY REPORT

FOR

MAX4173HExx

PLASTIC ENCAPSULATED DEVICES

December 18, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4173H successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4173H low-cost, precision, high-side current-sense amplifier is available in a tiny SOT23-6 package. It features a voltage output that eliminates the need for gain-setting resistors and it is ideal for today's notebook computers, cell phones, and other systems where current monitoring is critical. High-side current monitoring is especially useful in battery-powered systems, since it does not interfere with the ground path of the battery charger. The input common-mode range of 0 to +28V is independent of the supply voltage and ensures that the current-sense feedback remains viable even when connected to a battery in deep discharge. The MAX4173H's wide 1.7MHz bandwidth makes it suitable for use inside battery charger control loops.

The MAX4173H operates from a single +3V to +28V supply, typically draws only 420µA of supply current over the extended operating temperature range (-40°C to +85°C), and is offered in the space-saving SOT23-6 package.

B. Absolute Maximum Ratings

Item	Rating
VCC, RS+, RS- to GND	-0.3V to +30V
OUT to GND	-0.3V to (VCC + 0.3V)
Output Short-Circuit to VCC or GND	Continuous
Differential Input Voltage (VRS+ - VRS-)	±0.3V
Current into Any Pin.	±20mA
Continuous Power Dissipation (TA = +70°C)	
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-pin SOT23	696mW
8-pin NSO	471mW
Derates above +70°C	
6-pin SOT23	8.7mW/°C
8-pin NSO	5.88mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, SOT23, Voltage-Output, High-Side Current-Sense Amplifier
B. Process:	S12 – Silicon Gate 1.2 micron CMOS
C. Number of Device Transistors:	187
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**6-Lead SOT23**	**8-Lead NSO**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Bonding Diagram	#05-3001-0135	#05-3001-0122
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	44 x 38 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times \underbrace{4389}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}} \times 160 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

$\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5352) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP81-2 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4173HExx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23 NSO	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

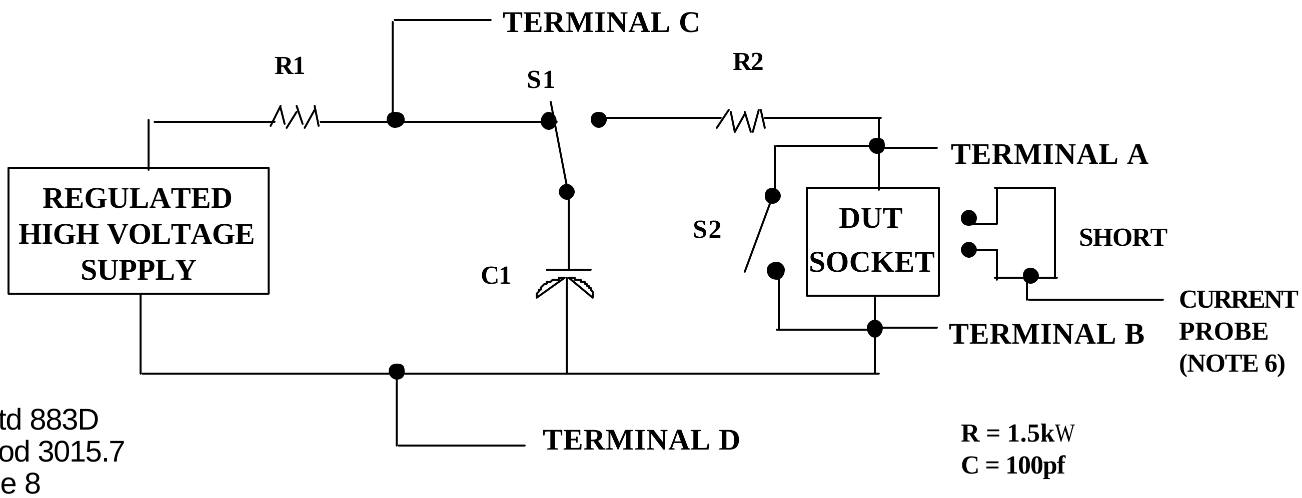
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

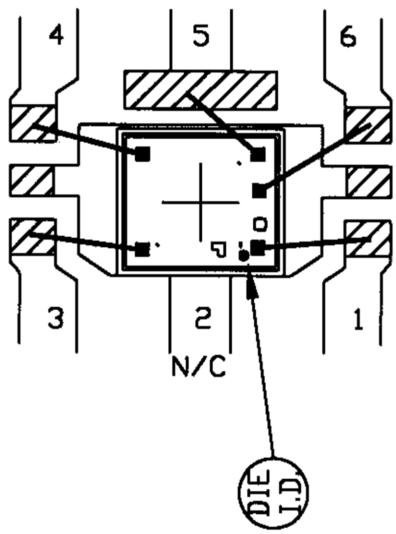
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

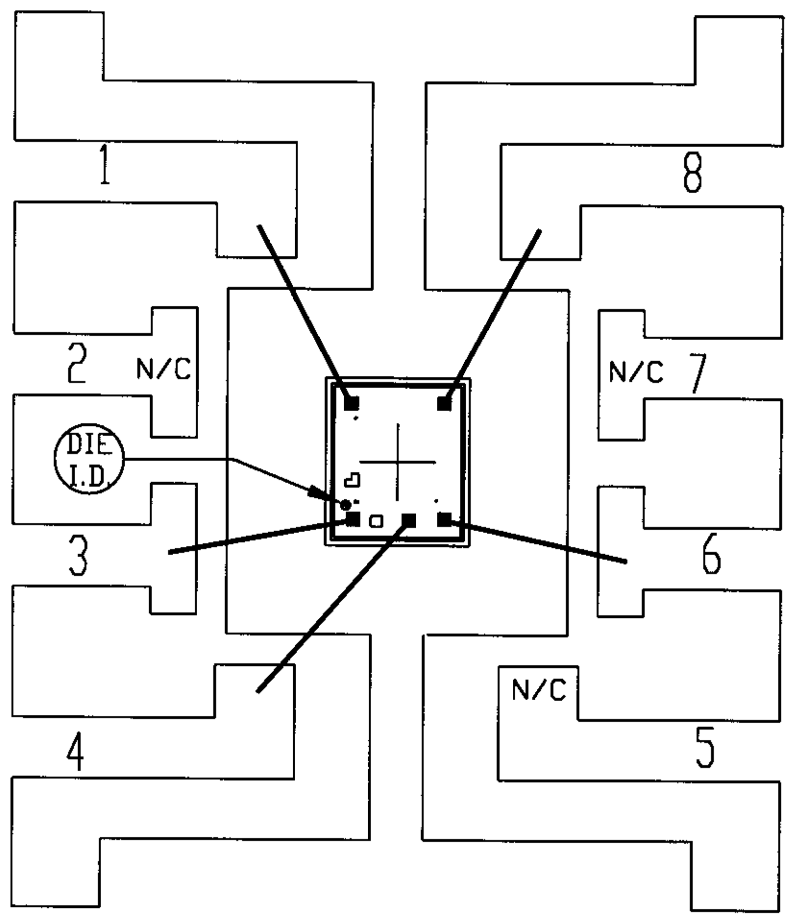
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





NOTE: CAVITY DOWN

PKG.CODE: U6-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 64x39	PKG. DESIGN			BUILDSHEET NUMBER: 05-3001-0135	REV.: A

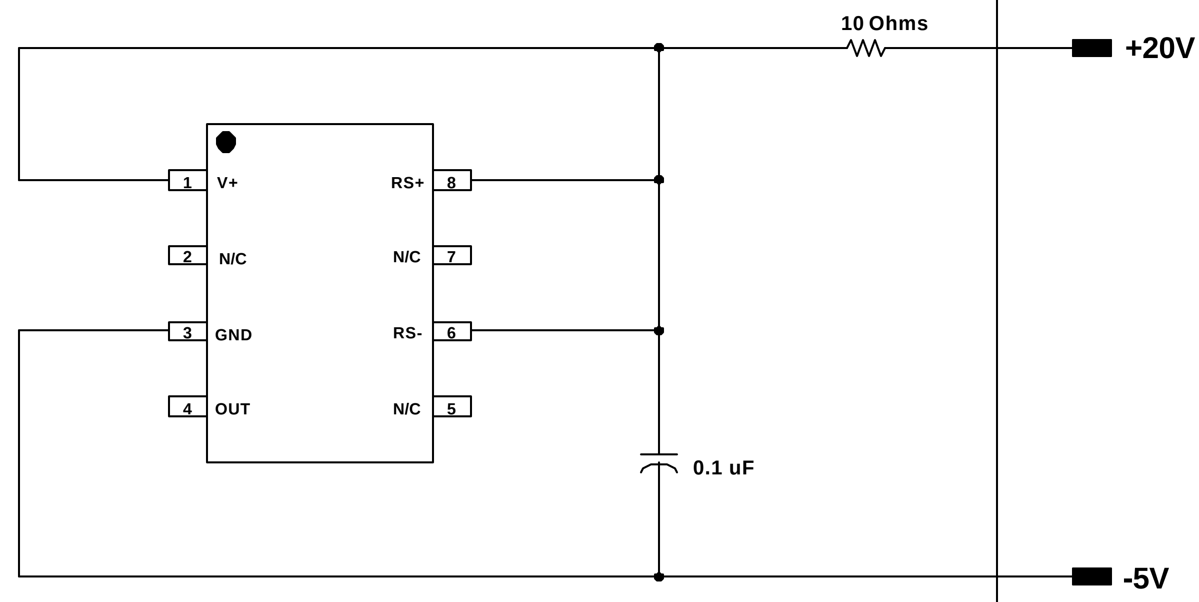


PKG.CODE: S8-2		APPROVALS	DATE
CAV./PAD SIZE: 90 X 90	PKG. DESIGN		

MAXIM

BUILDSHEET NUMBER:	REV.:
05-3001-0122	A

ONCE PER SOCKET | **ONCE PER BOARD**



DEVICES: MAX 4376/4173/4372
PACKAGE: 8-NSO
MAX. EXPECTED CURRENT = 60uA

DRAWN BY: **TEK TAN**
NOTES: