RELIABILITY REPORT

FOR

MAX4272ESA

PLASTIC ENCAPSULATED DEVICES

July 29, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4272 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4272 is an integrated 3V to 12V hot swap controllers allowing the safe insertion and removal of circuit cards into live backplanes.

The discharged filter capacitors of the circuit card provides a low impedance to the live backplane. High in-rush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. This family of hot swap controllers prevents such problems by regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide DualSpeed/BiLevel™ protection against short circuits, load glitches, and overcurrent conditions. In the event of a fault condition, the load is disconnected. Fault recovery is handled autoretry.

The MAX4272 includes many integrated features that reduce component count and design time. An on-board charge pump provides the gate drive for a low-cost, external N-FET. Integrated features like startup current regulation and current glitch protection eliminate external timing resistors and capacitors. Also featured are an open-drain status output to indicate a fault condition, and an adjustable overcurrent response time.

The MAX4272 (autoretry fault protection) come in the space-saving 8-pin SO package. The part is specified across the extended temperature range, and has an absolute maximum rating of 15V to provide extra protection against inductive kickback during board removal.

B. Absolute Maximum Ratings

Item	Rating
IN to GND	+15V
STAT, OUTC, LLMON, AUXVCC to GND	-0.3V to +14V
GATE to GND	-0.3V to (VIN + 8.5V)
GATE to LLMON (Note 1)	-1V to +8.5V
INC, ON to GND (Note 2)	-1V to +14V
CEXT to GND	-8.5V to (VIN + 0.3V)
CSPD, CTON, REF to GND	-0.3V to the lower of (VIN + 0.3V) or +12V
VSENSE, RTH, CTIM to GND	-0.3V to (VIN + 0.3V)
Current into INC, ON (Note 2)	±2mA
Current into Any Other Pin	±50mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = 70°C)	
8-Pin SO	471mW
Derates above +70°C	
8-Pin SO	5.9mW/°C

Note 1: GATE can be pulled below LLMON, but current must be limited to 2mA.
Note 2: INC and ON can be pulled below ground. Limiting the current to 2mA ensures that these pins are never lower than about -0.8V.

II. Manufacturing Information

A. Description/Function:	3V to 12V Current-Limiting Hot Controllers with Autoretry, DualSpeed/BiLevel Fault Protection
B. Process:	S3 [(SG3) - Standard 3 micron silicon gate CMOS]
C. Number of Device Transistors:	1685
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	April, 2000

III. Packaging Information

A. Package Type:	**8 Lead SO**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-3001-0172
H. Flammability Rating:	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	87 x 145 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager of Reliability Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 29.97 \times 10^{-9}$ $\lambda = 29.97$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5452) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP00-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4272ESA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	80	1
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

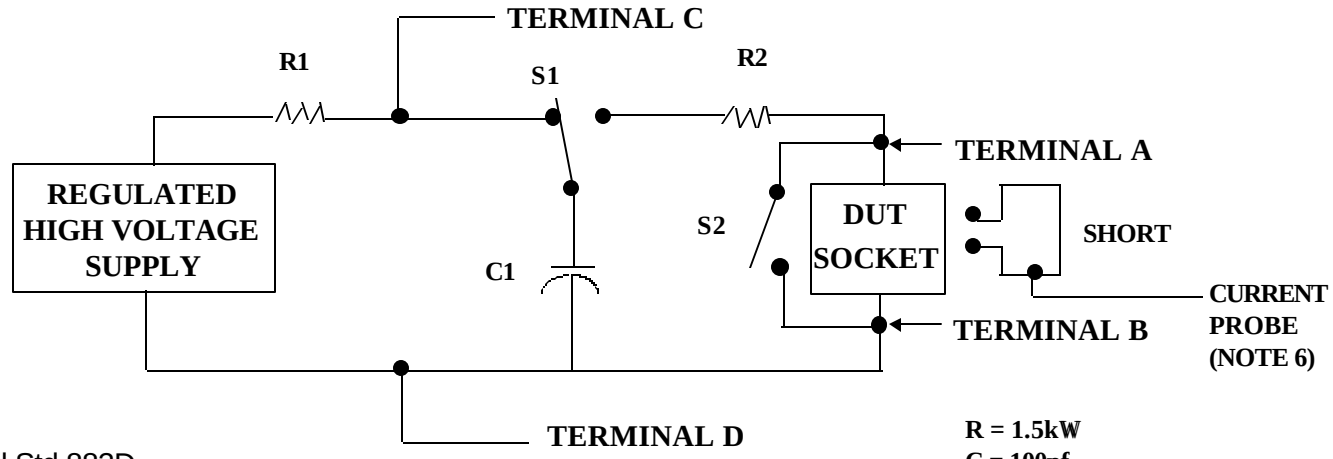
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

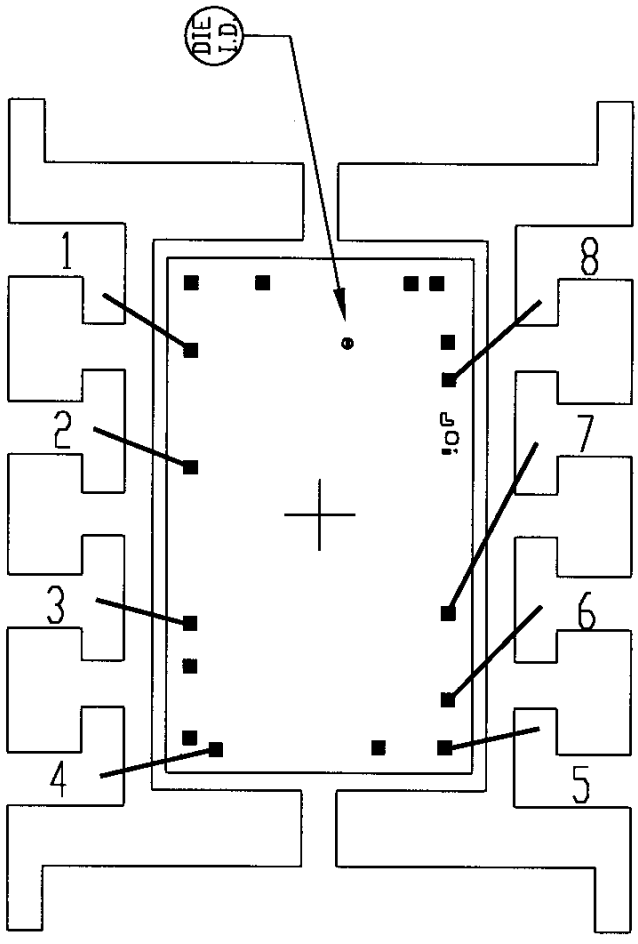
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

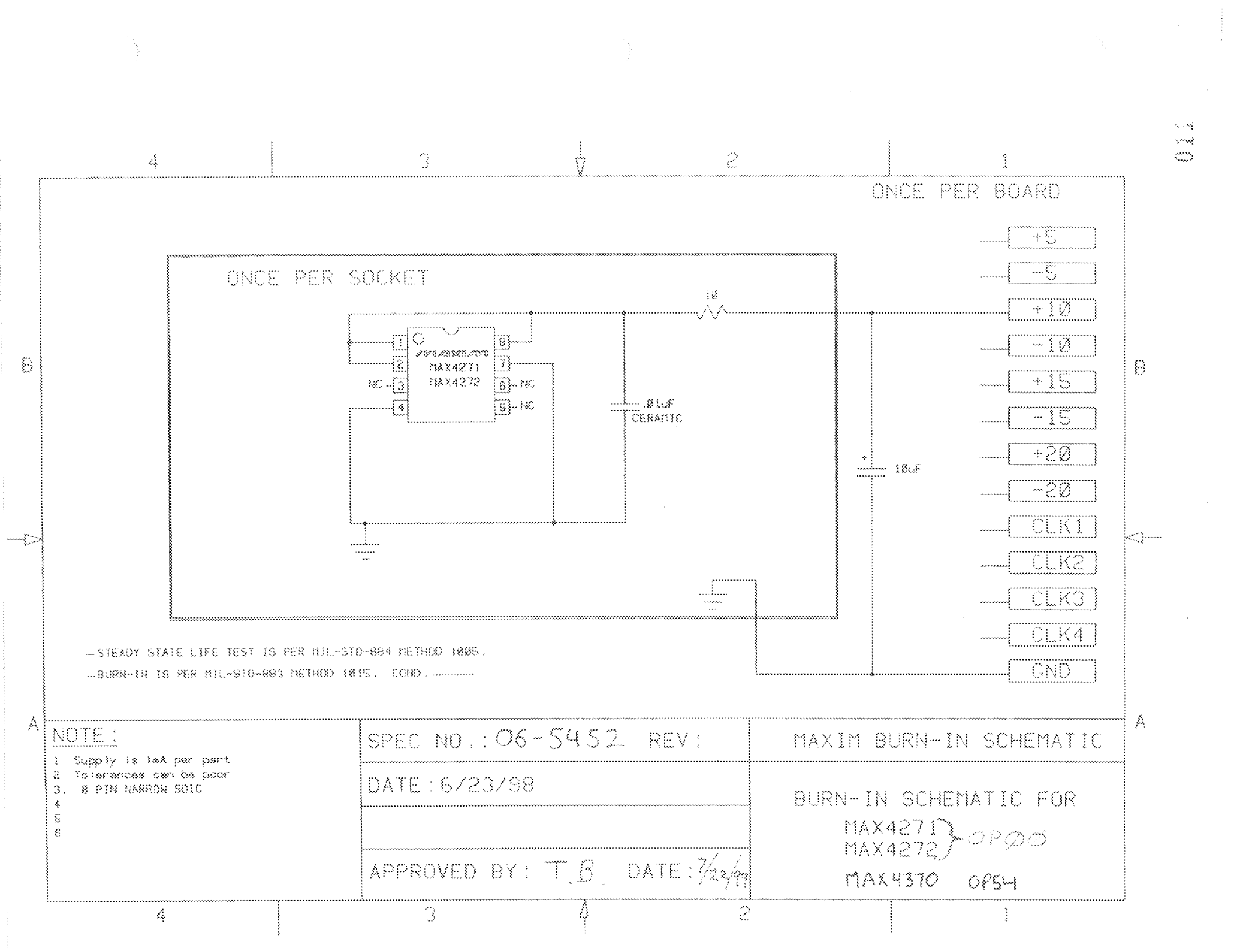
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: S8-5		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 95 X 155	PKG. DESIGN			BOND DIAGRAM #: 05-3001-0172	REV: A


ONCE PER BOARD
ONCE PER SOCKET
MAX4271
MAX4272
NC
.01uF
CERAMIC
10uF
+5
-5
+10
-10
+15
-15
+20
-20
CLK1
CLK2
CLK3
CLK4
GND
—STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
—BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. ———
NOTE:
1 Supply is 1mA per part
2 Tolerances can be poor
3. 8 PIN NARROW SOIC
SPEC NO.: 06-5452 REV:
DATE: 6/23/98
APPROVED BY: T.B. DATE: 7/23/98
MAXIM BURN-IN SCHEMATIC
BURN-IN SCHEMATIC FOR
MAX4271
MAX4272
OP05
MAX4370 OP54