RELIABILITY REPORT

FOR

MAX4370ESA

PLASTIC ENCAPSULATED DEVICES

January 27, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4370 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4370 is a circuit-breaker IC designed to offer protection in hot-swap applications using Maxim's DualSpeed/BiLevel™ detection. This controller, designed to reside either on the backplane or on the removable card, is used to protect a system from start-up damage when a card or board is inserted into a rack with the main system power supply turned on. The card's discharged filter capacitors provide a low impedance that can momentarily cause the main power supply to collapse. The MAX4370 prevents this start-up condition by providing inrush current regulation during a programmable start-up period, allowing the system to stabilize safely. In addition, two on-chip comparators provide DualSpeed/BiLevel short-circuit protection and overcurrent protection during normal operation.

The MAX4370 provides protection for a +3V to +12V single supply. An internal charge pump generates the controlled gate drive for an external N-channel MOSFET power switch. The MAX4370 latches the switch off after a fault condition until an external reset signal clears the device. Other features include a status pin to indicate a fault condition, an adjustable overcurrent response time, and a power-on reset comparator.

The MAX4370 is specified for the extended-industrial temperature range (-40°C to +85°C) and is available in an 8-pin SO package.

B. Absolute Maximum Ratings

Item	Rating
Vin to GND	+15V
STAT to GND	-0.3V t0 +14V
GATE to Gnd	-0.3V to (VIN + 8.5V)
ON to GND (Note 1)	-1V to +14V
CSPD to GND	-0.3V to the lower of (VIN + 0.3V) or +12V
VSEN, CTIM to GND	-0.3V to (VIN + 0.3V)
Current into ON	+/-2mA
Current inot any other Pin	+/-50mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continous Power Dissipation (T_A = +70^{0}C)	
8-Lead SO	471mW
Derates above +70°C	
8-Lead SO	5.9mW/°C

II. Manufacturing Information

A. Description/Function:	Current-Regulating Hot-Swap Controller with DualSpeed/BiLevel Fault Protection
B. Process:	S3 (SG3) Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	1792
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Phillipines or Thailand
F. Date of Initial Production:	April, 1999

III. Packaging Information

A. Package Type:	**8-Lead NSO**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3001-0143
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	87 x 145 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5452) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP54 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4370ESA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	9
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	2340	18
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

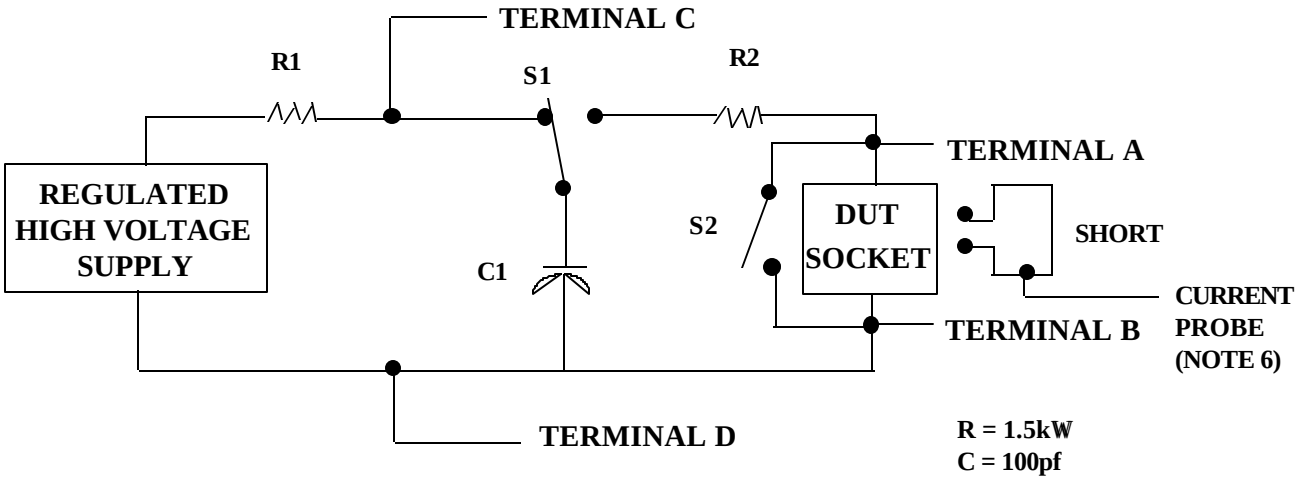
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

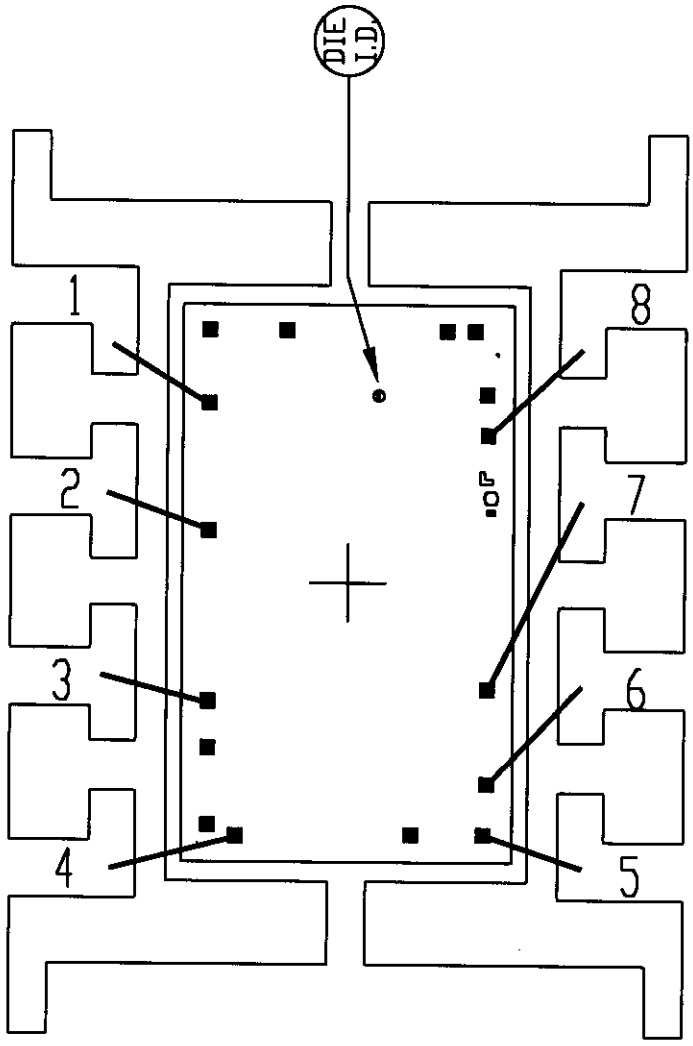
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

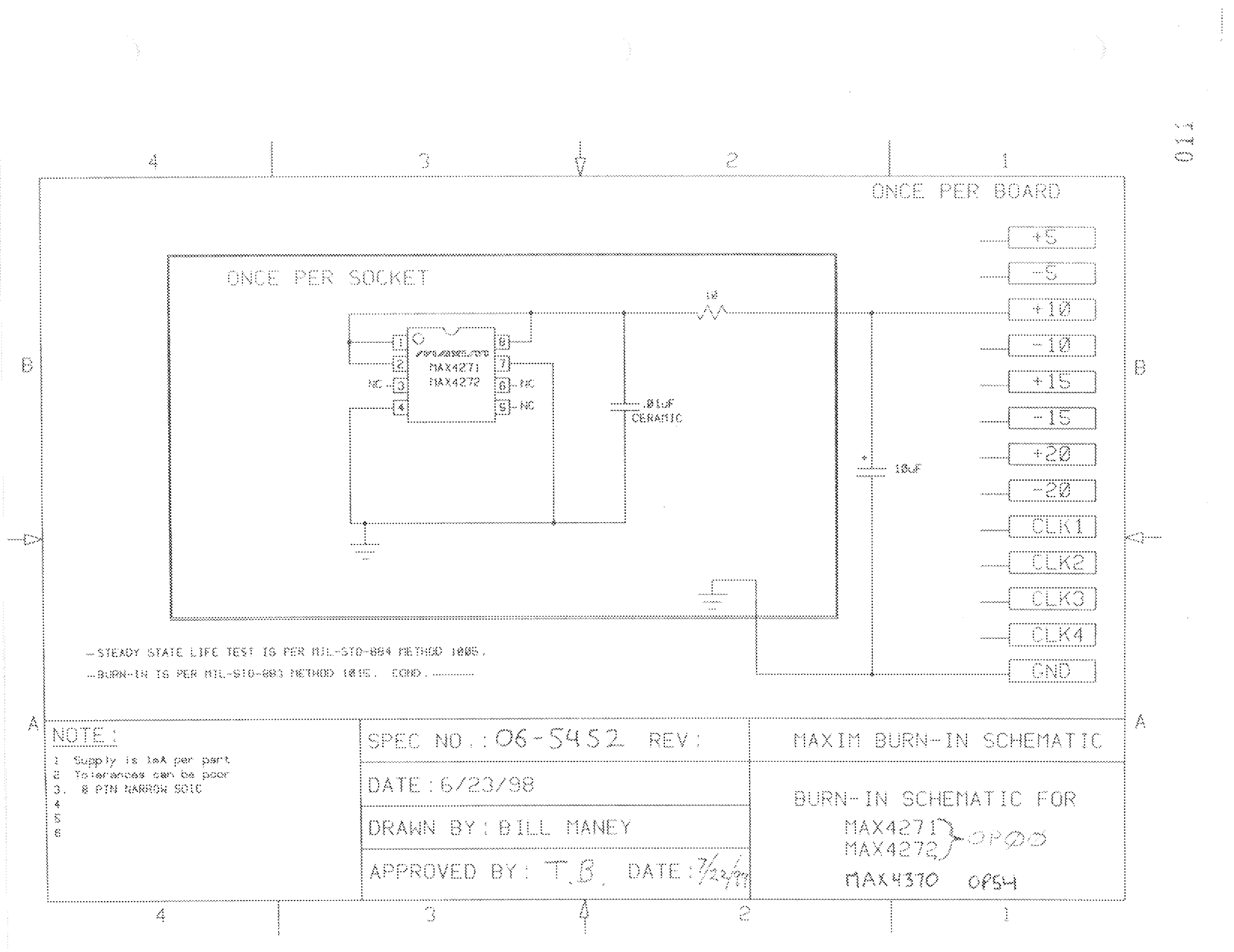
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-5		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 95 X 155	PKG. DESIGN			BUILDSHEET NUMBER: 05-3001-0143 / REV.: A


ONCE PER BOARD
ONCE PER SOCKET
MAX4271
MAX4272
NC
.01uF
CERAMIC
10uF
+5
-5
+10
-10
+15
-15
+20
-20
CLK1
CLK2
CLK3
CLK4
GND
—STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
—BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. ———
NOTE:
1 Supply is 1mA per part
2 Tolerances can be poor
3. 8 PIN NARROW SOIC
4
5
6
SPEC NO.: 06-5452 REV:
DATE: 6/23/98
DRAWN BY: BILL MANEY
APPROVED BY: T.B. DATE: 7/23/98
MAXIM BURN-IN SCHEMATIC
BURN-IN SCHEMATIC FOR
MAX4271
MAX4272
OP90
MAX4370 OP54