RELIABILITY REPORT

FOR

**MAX4375TExx**

PLASTIC ENCAPSULATED DEVICES

July 26, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

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**Conclusion**

The MAX4375T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



## I. Device Description

### A. General

The MAX4375T low-cost, micropower, high-side current-sense supervisor contains a high-side current-sense amplifier, bandgap reference, and comparator with latching output. It features a voltage output that eliminates the need for gain-setting resistors, making it ideal for today's notebook computers, cell phones, and other systems where battery/DC current monitoring is critical. High-side current monitoring is especially useful in battery-powered systems since it does not interfere with the ground path of the battery charger. The 0 to +28V input common-mode range is independent of the supply voltage, which ensures that the current-sense feedback remains viable even when connected to a battery pack in deep discharge.

The comparator output of the MAX4375T is latched to provide a turn-off flag that doesn't oscillate. In addition, the MAX4375T contain a second comparator for use in window-detection functions. The MAX4375T is available in three different gain versions (T = +20V/V, F = +50V/V, H = +100V/V) and use an external sense resistor to set the sensitivity of the input voltage to the load current. These features offer a high level of integration, resulting in a simple and compact current-sense solution.

The MAX4375T operates from a single +2.7V to +28V supply and consumes 50µA. It is specified for the extended operating temperature range (-40°C to +85°C) and is available in 10-pin µMAX packages.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| VCC, RS+, RS- to GND | -0.3V to +30V |
| OUT to GND | -0.3V to the lesser of (VCC + 0.3V) or +15V |
| CIN1, CIN2, RESET to GND | -0.3V to the lesser of (VCC + 0.3V) or +12V |
| Differential Input Voltage (VRS+ - VRS-) | ±0.3V |
| COUT1, COUT2 to GND | -0.3V to +6.0V |
| Current into Any Pin | ±10mA |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C | |
| 10-Pin µMAX | 444mW |
| 14-Pin SO | 667mW |
| Derates above +70°C | |
| 10-Pin µMAX | 5.6mW/°C |
| 14-Pin SO | 8.3mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Micropower High-Side Current-Sense Amplifier + Comparator + Reference ICs |
| B. Process: | S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS |
| C. Number of Device Transistors: | 390 |
| D. Fabrication Location: | Cailfornia or Oregon, USA |
| E. Assembly Location: | Malaysia, Philippines or Thailand |
| F. Date of Initial Production: | February, 2000 |

## III. Packaging Information

| | **10-Lead uMAX** | **14-Lead SO** |
|---|---|---|
| A. Package Type: | | |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1 mil dia.) | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | Buildsheet # 05-3001-0155 | Buildsheet # 05-3001-0153 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 55 x 64 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Copper/Si |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec. # 06-5435) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP86-6 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX4375TExx**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | uMAX<br>SO | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

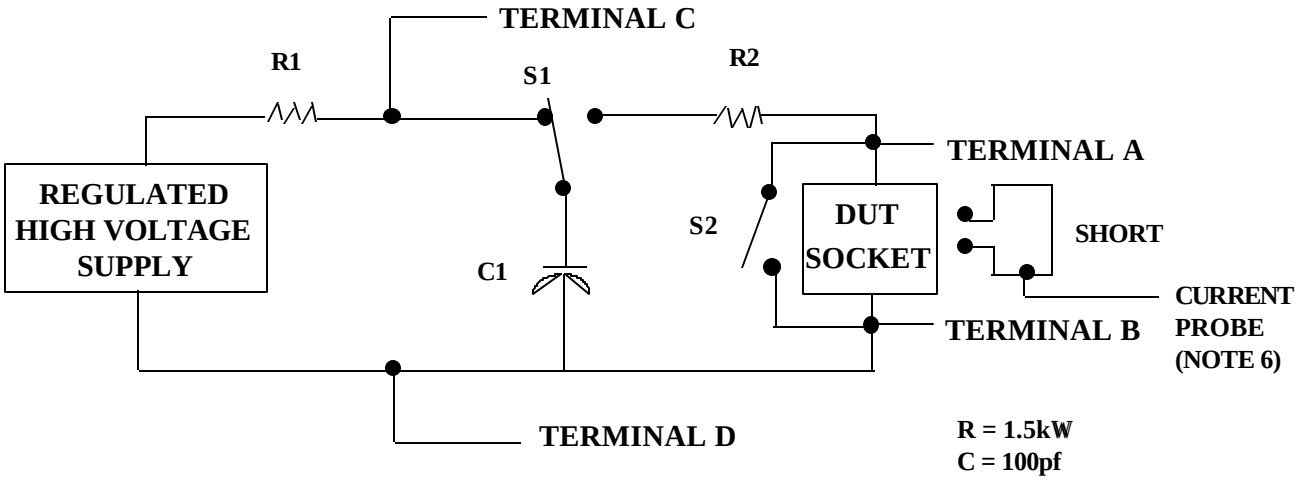
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

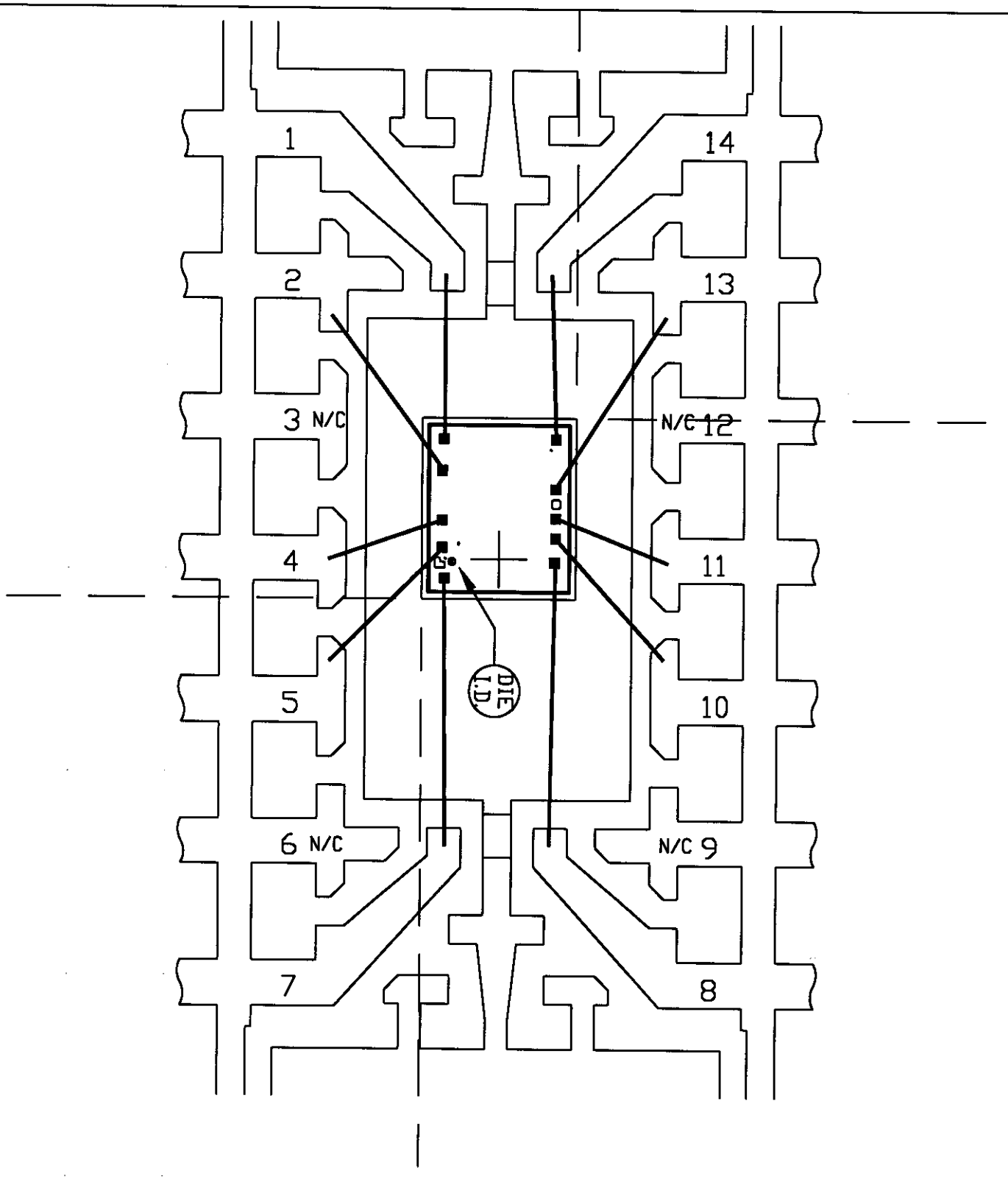
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

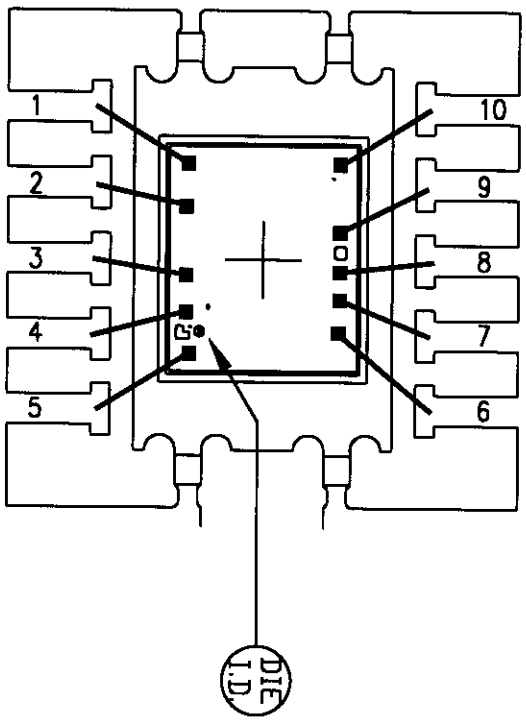
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



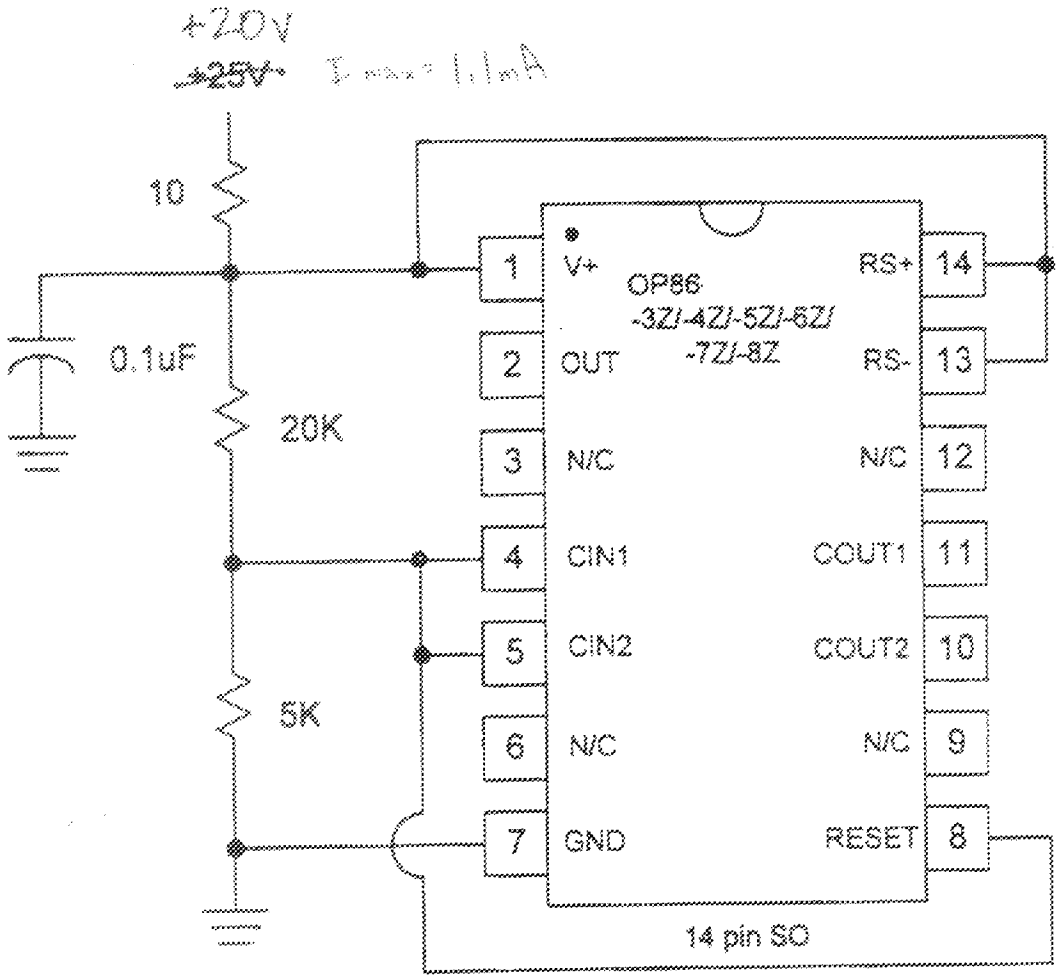



| | | | | |
|---|---|---|---|---|
| PKG.CODE: S14-4 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 95X170 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-3001-0153 / REV.: A |




| | | | | |
|---|---|---|---|---|
| PKG.CODE: U10-2 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 68X94 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-3001-0155 / REV.: A |

06-5435




BURN-IN SCHEMATIC
MAX4374T/5T ESD
MAX4374F/5F ESD
MAX4374H/5H ESD
14 PIN SOIC
2.8mW DISSIPATION