

RELIABILITY REPORT
FOR
MAX44205ATC+T
PLASTIC ENCAPSULATED DEVICES

March 25, 2015

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering

Conclusion

The MAX44205ATC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX44205 is a low-noise, low-distortion fully differential operational amplifier suitable for driving high-speed, high-resolution, 20-/18-/16-bit SAR ADCs, including the MAX11905 ADC family. Featuring a combination of wide 2.7V to 13.2V supply voltage range and wide 400MHz bandwidth, the MAX44205 is suitable for low-power, high-performance data acquisition systems. The MAX44205 offers a V_{OCM} input to adjust the output common-mode voltage, eliminating the need for a coupling transformer or AC-coupling capacitors. This adjustable output common-mode voltage allows the MAX44205 to match the input common-mode voltage range of the ADC following it. A proprietary output voltage clamping solution ensures that the buffer output does not violate the ADC's maximum input voltage range, even if the MAX44205's supply rails are higher than the ADC's full-scale range. Shutdown mode consumes only 6.8 μ A and extends battery life in battery-powered applications or reduces average power in systems cycling between shutdown and periodic data readings. The MAX44205 is available in 12-pin, 3mm x 3mm, TQFN and 10-pin μ MAX® packages and is specified for operation over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	180MHz, Low-Noise Fully Differential SAR ADC Driver	
B. Process:	CB5	
C. Fabrication Location:	USA	
D. Assembly Location:	USA, Taiwan, China, Thailand	USA, Philippines, Thailand
E. Date of Initial Production:	June 27, 2014	

III. Packaging Information

A. Package Type:	12-pin TQFN 3x3	10-pin uMAX
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5535	#05-9000-5536
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	76°C/W	97°C/W
K. Single Layer Theta Jc:	10.8°C/W	5°C/W
L. Multi Layer Theta Ja:	68°C/W	77.6°C/W
M. Multi Layer Theta Jc:	11°C/W	5°C/W

IV. Die Information

A. Dimensions:	59.8425 X 59.8425 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.4 microns (as drawn)
G. Isolation Dielectric:	SiO ₂
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.9 \times 10^{-9}$$

$$\lambda = 13.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the Process results in a FIT Rate of 0.88 @ 25°C and 15.16 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OZ02-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX44205ATC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.