

RELIABILITY REPORT  
FOR  
MAX44241AUA+T  
PLASTIC ENCAPSULATED DEVICES

September 8, 2014

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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## Conclusion

The MAX44241AUA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX44241/MAX44243/MAX44246 are 36V, ultra-precision, low-noise, low-drift, single/quad/dual operational amplifiers that offer near-zero DC offset and drift through the use of patented chopper stabilized and auto-zeroing techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. These single/quad/dual devices feature rail-to-rail outputs, operate from a single 2.7V to 36V supply or dual  $\pm 1.35V$  to  $\pm 18V$  supplies, and consume only 0.42mA per channel, with only 9nV/ input-referred voltage noise. The ICs are unity-gain stable with a gain-bandwidth product of 5MHz. With excellent specifications such as offset voltage of 5 $\mu V$  (max), drift of 20nV/ $^{\circ}C$  (max), and 117nVP-P noise in 0.1Hz to 10Hz, these ICs are ideally suited for applications requiring ultra-low noise, and DC precision such as interfacing with pressure sensors, strain gauges, precision weight scales, and medical instrumentation. The ICs are available in 8-pin  $\mu MAX^{\circ}$  or SO packages and are rated over the  $-40^{\circ}C$  to  $+125^{\circ}C$  temperature range.

## II. Manufacturing Information

A. Description/Function:	36V, Low-Noise, Precision, Single/Quad/Dual Op Amps
B. Process:	S18
C. Number of Device Transistors:	597
D. Fabrication Location:	USA
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	November 11, 2013

## III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5345
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	41.9°C/W

## IV. Die Information

A. Dimensions:	48.4252 X 31.4961 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot EALQ0Q001A, D/C 1319)

The OY91-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78

With the following exceptions:

OUT pin passes +100mA/-80mA per JEDEC JESD78

**Table 1**  
Reliability Evaluation Test Results  
MAX44241AUA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SAFB4Q001D, D/C 1213

Note 1: Life Test Data may represent plastic DIP qualification lots.