RELIABILITY REPORT

FOR

MAX44243AUD+T

PLASTIC ENCAPSULATED DEVICES

July 26, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX44243AUD+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX44241/MAX44243/MAX44246 are 36V, ultra- precision, low-noise, low-drift, single/quad/dual opera- tional amplifiers that offer near-zero DC offset and drift through the use of patented chopper stabilized and auto-zeroing techniques. This method constantly mea- sures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. These single/quad/dual devices feature rail-to-rail out- puts, operate from a single 2.7V to 36V supply or dual ±1.35V to ±18V supplies, and consume only 0.42mA per channel, with only 9nV/ Hz input-referred voltage noise. The ICs are available in 8-pin µMAX® or SO packages and are rated over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	36V, Low-Noise, Precision, Single/Quad/Dual Op Amps
B. Process:	S18
C. Number of Device Transistors:	1234
D. Fabrication Location:	USA
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	November 11, 2013

III. Packaging Information

A. Package Type:	14-pin TSSOP	14-pin SOIC
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (0.8 mil dia.)	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#31-4915	#31-4916
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	110°C/W	120°C/W
K. Single Layer Theta Jc:	30°C/W	37°C/W
L. Multi Layer Theta Ja:	100.4°C/W	81°C/W
M. Multi Layer Theta Jc:	30°C/W	32°C/W

IV. Die Information

A. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
B. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
C. Backside Metallization:	None
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Bondpad Dimensions:	
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 318 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.5 \times 10^{-9}$

$\lambda = 3.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OZ03-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX44243AUD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	318	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.