

RELIABILITY REPORT

FOR

MAX44285

PLASTIC ENCAPSULATED DEVICES

February 10, 2017

MAXIM INTEGRATED

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Conclusion

The MAX44285 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX44285 dual-channel high-side current-sense amplifier has precision accuracy specifications of VOS less than 10µV (max) and gain error less than 0.1% (max). The MAX44285 features an input common-mode voltage range from 2.7V to 76V with 80kHz of small-signal bandwidth, which makes it ideal for interfacing with a SAR ADC for multichannel multiplexed data acquisition systems. The MAX44285 operates over the -40°C to +125°C temperature range. The MAX44285 is offered in 8-bump WLP and 8-pin µMAX® packages.



II. Manufacturing Information

A. Description/Function:	Dual-Channel, High-Precision, High-Voltage, Current-Sense Amplifier
B. Process:	S18
C. Number of Device Transistors:	10565
D. Fabrication Location:	USA
E. Assembly Location:	Philippines, Thailand USA
F. Date of Initial Production:	February 3, 2014

III. Packaging Information

A. Package Type:	8-pin uMAX	8-bump WLP
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-5341	#05-9000-5342
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C 	Level 1	Level 1
J. Single Layer Theta Ja:	221°C/W	N/A°C/W
K. Single Layer Theta Jc:	42°C/W	N/A°C/W
L. Multi Layer Theta Ja:	206.3°C/W	75°C/W
M. Multi Layer Theta Jc:	42°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	83.8582 X 43.7008 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	AI/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:D. Sampling Plan:	< 50 ppm Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (A) is calculated as follows:

 $\frac{1}{MTF} = \frac{1}{102 \times 4340 \times 160 \times 2}$ (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

𝔅 = 6.87 x 10⁻⁹

x = 6.87 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OY94 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX44285

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test	(Note 1)				
	Ta = 135°C	DC Parameters	160	0	
	Biased	& functionality			
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.