

RELIABILITY REPORT  
FOR  
MAX4475ATT+T  
PLASTIC ENCAPSULATED DEVICES

March 24, 2011

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

|                      |
|----------------------|
| <b>Approved by</b>   |
| Sokhom Chum          |
| Quality Assurance    |
| Reliability Engineer |

## Conclusion

The MAX4475ATT+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4475-MAX4478/MAX4488/MAX4489 wideband, low-noise, low-distortion operational amplifiers offer rail-to-rail outputs and single-supply operation down to 2.7V. They draw 2.2mA of quiescent supply current per amplifier while featuring ultra-low distortion (0.0002% THD+N), as well as low input voltage-noise density (4.5nV/√) and low input current-noise density (0.5fA). These features make the devices an ideal choice for applications that require low distortion and/or low noise. For power conservation, the MAX4475/MAX4488 offer a low-power shutdown mode that reduces supply current to 0.01μA and places the amplifiers' outputs into a high-impedance state. These amplifiers have outputs which swing rail-to-rail and their input common-mode voltage range includes ground. The MAX4475-MAX4478 are unity-gain stable with a gain-bandwidth product of 10MHz. The MAX4488/4489 are internally compensated for gains of +5V/V or greater with a gain-bandwidth product of 42MHz. The single MAX4475/MAX4476/MAX4488 are available in space-saving, 6-pin SOT23 and TDFN packages.

**II. Manufacturing Information**

|                                  |   |
|----------------------------------|---|
| A. Description/Function:         | SOT23, Low-Noise, Low-Distortion, Wide-Band, Rail-to-Rail Op Amps |
| B. Process:                      | B12   |
| C. Number of Device Transistors: |   |
| D. Fabrication Location:         | Oregon  |
| E. Assembly Location:            | Thailand  |
| F. Date of Initial Production:   | July 28, 2001   |

**III. Packaging Information**

|  |                          |
|--|--------------------------|
| A. Package Type:   | 6-pin TDFN 3x3           |
| B. Lead Frame:   | Copper                   |
| C. Lead Finish:  | 100% matte Tin           |
| D. Die Attach:   | Conductive               |
| E. Bondwire:   | Au (1 mil dia.)          |
| F. Mold Material:  | Epoxy with silica filler |
| G. Assembly Diagram:   | #05-2501-0146            |
| H. Flammability Rating:  | Class UL94-V0            |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1                  |
| J. Single Layer Theta Ja:  | 55°C/W                   |
| K. Single Layer Theta Jc:  | 9.0°C/W                  |
| L. Multi Layer Theta Ja:   | 42°C/W                   |
| M. Multi Layer Theta Jc:   | 9.0°C/W                  |

**IV. Die Information**

|                            |   |
|----------------------------|---|
| A. Dimensions:             | 45 X 87 mils  |
| B. Passivation:            | Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide) |
| C. Interconnect:           | Al/0.5%Cu with Ti/TiN Barrier   |
| D. Backside Metallization: | None  |
| E. Minimum Metal Width:    | 1.2 microns (as drawn)  |
| F. Minimum Metal Spacing:  | 1.2 microns (as drawn)  |
| G. Bondpad Dimensions:     | 5 mil. Sq.  |
| H. Isolation Dielectric:   | SiO <sub>2</sub>  |
| I. Die Separation Method:  | Wafer Saw   |

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 30.3 \times 10^{-9}$$

$$\lambda = 30.3 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.06 @ 25C and 1.06 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot J3J0EQ003D D/C 0846)

The OX48 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX4475ATT+T**

| TEST ITEM                        | TEST CONDITION                          | FAILURE IDENTIFICATION           | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS             |
|----------------------------------|---|----------------------------------|-------------|--------------------|----------------------|
| <b>Static Life Test</b> (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80          | 1                  | I3J0BQ002A, D/C 0130 |

Note 1: Life Test Data may represent plastic DIP qualification lots.