RELIABILITY REPORT

FOR

MAX4490AxK

PLASTIC ENCAPSULATED DEVICES

Aug 1, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX4490 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4490 single, low-cost CMOS op amp features Rail-to-Rail® input and output capability from either a single +2.7V to +5.5V supply or dual ±1.35V to ±2.75V supplies. This amplifier exhibita a high-performance slew rate of 10V/µs and a gain-bandwidth product of 10MHz. It can drive 2kΩ resistive loads to within 55mV of either supply rail and remain unity-gain stable with capacitive loads up to 200pF.

The MAX4490 is offered in the ultra-small, 5-pin SC70 package, which is 50% smaller than the standard 5-pin SOT23 package. Specifications the part is guaranteed over the automotive (-40°C to +125°C) temperature range.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VDD to VSS)	6V
All Other Pins	(VSS - 0.3V) to (VDD + 0.3V)
Output Short-Circuit Duration	10s
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
(Voltages Referenced to GND)	
Continuous Power Dissipation (TA = +70°C)	
5-Pin SC70	200mW
5-Pin SOT23	571mW
Derates above +70°C	
5-Pin SC70	2.5mW/°C
5-Pin SOT23	7.1mW/°C

Note 1: Signals on COM_, NO_ exceeding V+ or V- are clamped by internal diodes. A_ and EN are clamped only to V- and can exceed V+ up to their maximum ratings. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Low-Cost, High-Slew-Rate, Rail-to-Rail I/O Op Amps
B. Process:	TC05 (0.5 micron CMOS)
C. Number of Device Transistors:	60
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	July, 1999

III. Packaging Information

	5-Pin SC70	**5-Pin SOT23**
A. Package Type:		
B. Lead Frame:	Copper or Alloy 42	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-2501-0005	# 05-2401-0004
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	30 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.5 microns; Metal 2: 0.7 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.5 microns; Metal 2: 0.7 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 73 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 14.88 \times 10^{-9}$ $\lambda = 14.88$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5662) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OX27 die type has been found to have all pins able to withstand a transient pulse of +/-2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX4490AxK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		73	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT SC70	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

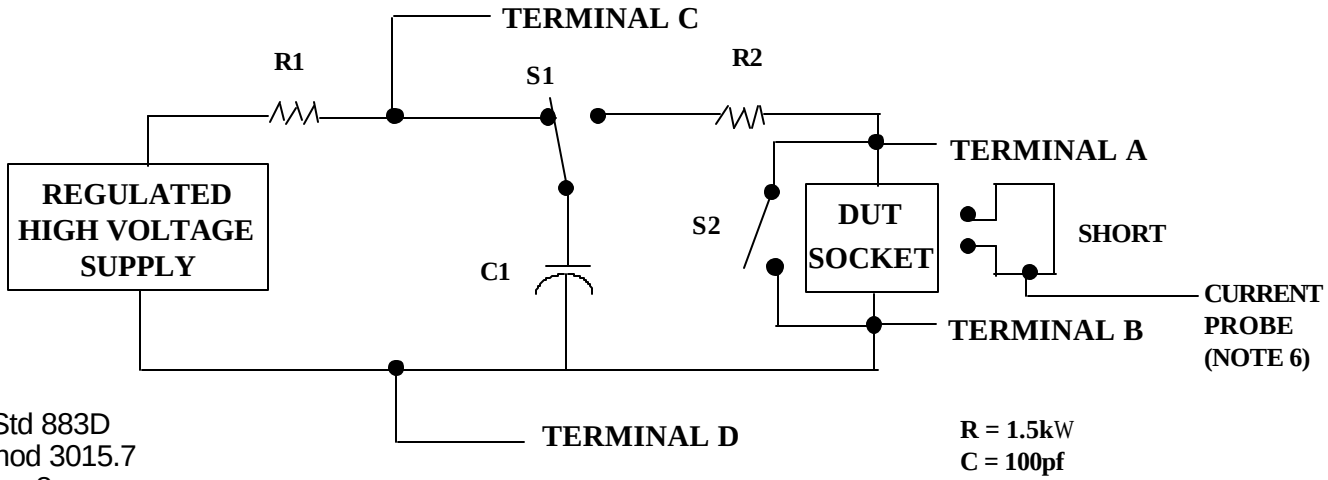
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

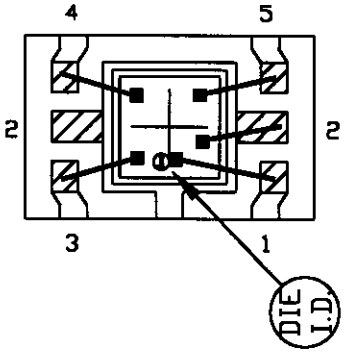
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



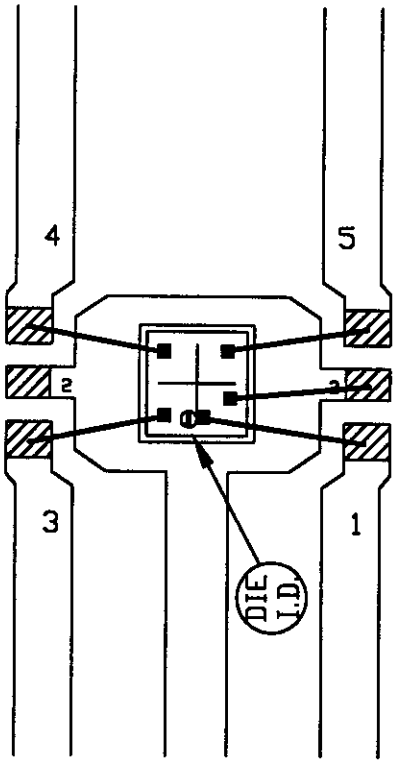
Mil Std 883D
Method 3015.7
Notice 8



▨ BONDABLE AREA

NOTE: CAVITY DOWN

PKG.CODE: X5-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 35x34	PKG. DESIGN			BUILDSHEET NUMBER: 05-2501-0005 / REV.: A



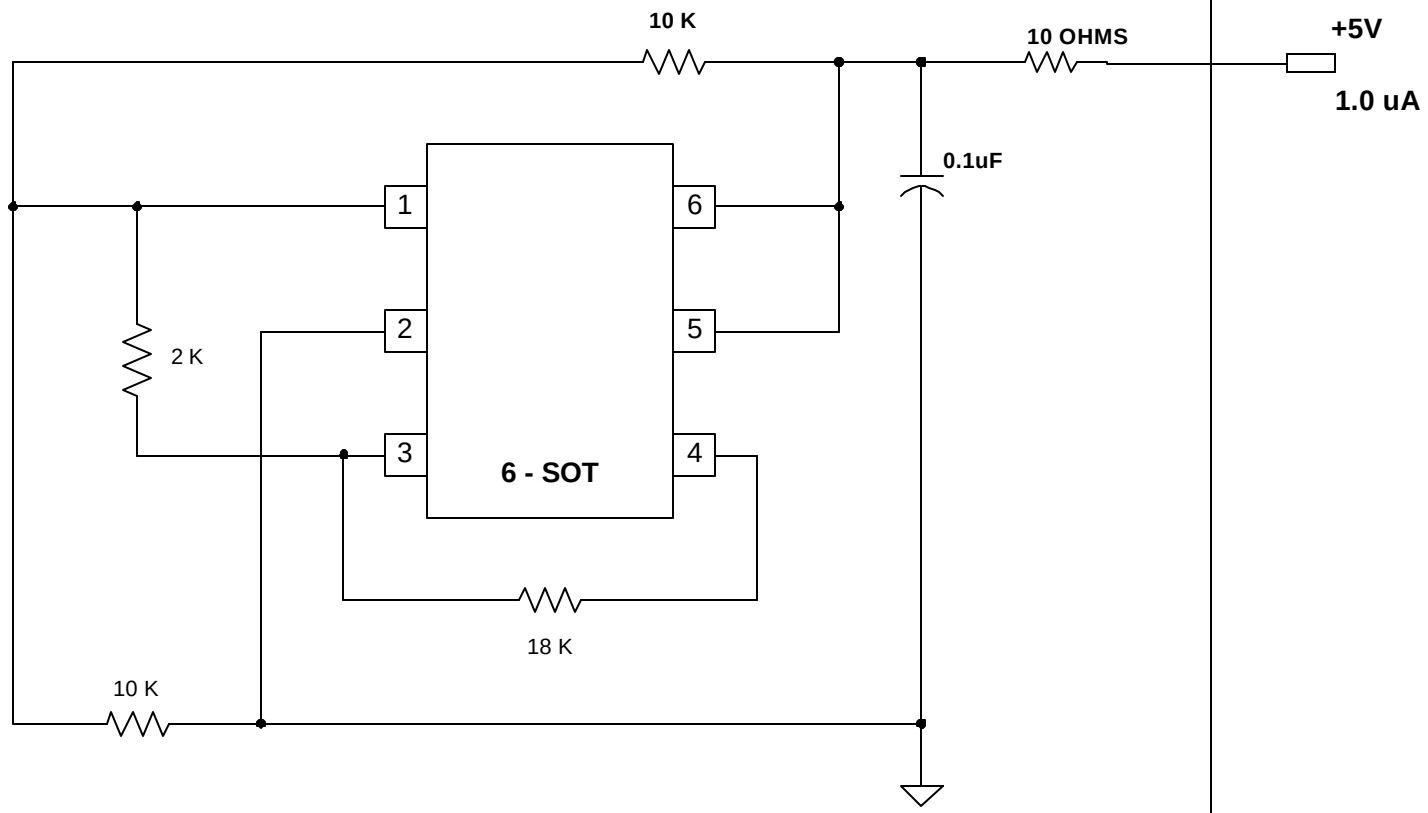
▨- BONDING AREA

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64X45	PKG. DESIGN			BUILDSHEET NUMBER: 05-2501-0004 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4464/4470/4400/4401/4480/4481/
4490/4291/4465/4466/4335/4336/4245/LMX321/4231
MAX CURRENT: MAX4481/MAX4291/LMX321= 800uA / MAX4464/4470/
4480/4465/4466= 400uA / MAX4400/4401/4245=1.2mA / MAX4490=2.5mA
MAX4435/4436/4231/4230=3.4mA