RELIABILITY REPORT

FOR

MAX5026EUT+

PLASTIC ENCAPSULATED DEVICES

July 9, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX5026EUT+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5025-MAX5028 constant-frequency, pulse-width modulating (PWM), low-noise boost converters are intended for low-voltage systems that often need a locally generated high voltage. These devices are capable of generating low-noise, high output voltages required for varactor diode biasing in TV tuners, set-top boxes, and PCI cable modems. The MAX5025-MAX5028 operate from as low as 3V and switch at 500kHz. The constant-frequency, current-mode PWM architecture provides for low output noise that is easy to filter. A 40V lateral DMOS device is used as the internal power switch, making the devices ideal for boost converters up to 36V. The MAX5025/MAX5026 adjustable versions require the use of external feedback resistors to set the output voltage. The MAX5027/MAX5028 offer a fixed 30V output. These devices are available in a small, 6-pin SOT23 package.

II. Manufacturing Information

A. Description/Function:	500kHz, 36V Output, SOT23, PWM Step-Up DC-DC Converters
B. Process:	BCD8
C. Number of Device Transistors:	366
D. Fabrication Location:	Oregon
E. Assembly Location:	Texas, Thailand
F. Date of Initial Production:	October 27, 2001

III. Packaging Information

A. Package Type:	6-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3601
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	115*°C/W
K. Single Layer Theta Jc:	80°C/W
L. Multi Layer Theta Ja:	74.6°C/W
M. Multi Layer Theta Jc:	6.1°C/W

IV. Die Information

A. Dimensions:	60 X 41 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 343 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.6 \times 10^{-9}$

λ = 0.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the BCD8 Process results in a FIT Rate of 0.04 @ 25C and 0.71 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot N3I0F2005C, D/C 1019)

The NP15 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5026EUT+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	J3I0E2012C, D/C 1007
	Biased	& functionality	80	0	N3I0F2003B, D/C 1007
	Time = 1000 hrs.		77	0	N3I0DA023C, D/C 0502
			54	0	J3I0E2011B, D/C 1007
			52	0	N3I0F2005C, D/C 1019

Note 1: Life Test Data may represent plastic DIP qualification lots.