RELIABILITY REPORT

FOR

MAX5048CAUT+T

PLASTIC ENCAPSULATED DEVICES

January 28, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX5048CAUT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5048C is a high-speed MOSFET driver capable of sinking/sourcing 7A/3A peak currents. This device takes logic input signals and drives a large external MOSFET. The device has inverting and noninverting inputs that give the user greater flexibility in controlling the MOSFET. The device also has the features necessary to drive low-side enhancement-mode Gallium Nitride (GaN) FETs. The device features two separate outputs working in complementary mode, offering flexibility in controlling both turn-on and turn-off switching speeds. The device has internal logic circuitry, which prevents shoot-through during output state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of V+ voltage. Propagation delay time is minimized and matched between the inverting and noninverting inputs. The device has very fast switching times combined with very short propagation delays (8ns typ) making it ideal for high-frequency circuits. The device operates from a +4V to +14V single power supply, typically consuming 0.5mA of supply current and has TTL input logic levels. This device is available in a 6-pin SOT23 package and provides an upgrade path for users of the MAX5048B.

II. Manufacturing Information

A. Description/Function:	7A Sink/3A Source Current, 8ns, SOT23, MOSFET Driver
B. Process:	S18
C. Number of Device Transistors:	666
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	November 29, 2012

III. Packaging Information

A. Package Type:	6-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4989
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	63.3858X24.8031 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23um
F. Minimum Metal Spacing:	0.23um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 90 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 12.2 \times 10^{-9}$

λ = 12.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.05 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAFV4Q001D, D/C 1235)

The PI18-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5048CAUT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	90	0	SAFV4Q001D, D/C 1235

Note 1: Life Test Data may represent plastic DIP qualification lots.