RELIABILITY REPORT

FOR

MAX5092BATE+

PLASTIC ENCAPSULATED DEVICES

July 9, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX5092BATE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5092A/MAX5092B/MAX5093A/MAX5093B low-quiescent-current, low-dropout (LDO) regulators contain simple boost preregulators operating at a high frequency. The devices seamlessly provide a preset 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B) LDO output voltage from an automotive cold-crank through load-dump (3.5V to 80V) input voltage conditions. The MAX5092_/MAX5093_ deliver up to 250mA with excellent load and line regulation. During normal operation, when the battery is healthy, the boost preregulator is completely turned off, reducing quiescent current to 65µA (typ). This makes the devices suitable for always-on power supplies. The buck-boost operation achieved by this combination of LDO and boost preregulator offers the advantage of using a single off-the-shelf inductor in place of the multiple- winding custom magnetics needed in typical single- ended primary inductor converter (SEPIC) and transformer-based flyback topologies. The high operating frequency of the boost regulator significantly reduces component size. The MAX5092_ integrates a blocking diode to further reduce the external component count. The boost preregulator output voltage is preset to 7V. Both LDO and boost output voltages are programmable using external resistors. The boost preregulator output voltage is adjustable up to 11V (MAX5092_), or up to 12V (MAX5093_). The LDO output voltage is adjustable from 1.5V to 9V (MAX5092_) or from 1.5V to 10V (MAX5093_). The devices feature a shutdown mode with 5µA (typ) shutdown current, a active-low HOLD input to implement a self-holding circuit, and a power-on-reset output (active-low RESET) with an externally programmable timeout period. Additional features include output overload, short-circuit, and thermal protection. The MAX5092_/MAX5093_ are available in a thermally enhanced, 16-pin 5mm x 5mm thin QFN package and can dissipate up to 2.7W at +70°C on a multilayer PC board.

II. Manufacturing Information

A. Description/Function:	4V to 72V Input LDOs with Boost Preregulator
B. Process:	BCD8
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	October 21, 2006

III. Packaging Information

A. Package Type:	16-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2077
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	30°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	130 X 135 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.4 \times 10^{-9}$

$\lambda = 23.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the BCD8 Process results in a FIT Rate of 0.04 @ 25C and 0.71@ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NN80BQ001C, D/C 0629)

The NP89 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX5092BATE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0	NN80BQ001C, D/C 0629

Note 1: Life Test Data may represent plastic DIP qualification lots.