RELIABILITY REPORT

FOR

MAX5120AEEE+

PLASTIC ENCAPSULATED DEVICES

December 11, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX5120AEEE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5120/MAX5121 are low-power, 12-bit, voltage-output digital-to-analog converters (DACs) with an internal precision bandgap reference and an output amplifier. The MAX5120 operates on a +5V supply with an internal amplifier reference of +2.5V and is capable of a +4.095V full-scale output range. The MAX5121, operating on +3V, delivers its +2.0475V full-scale output with an internal precision reference of +1.25V. If necessary, the user can override the internal, < 10ppm/°C voltage reference with an external reference. Both devices draw only 500µA of supply current, which reduces to 3µA in power-down mode. In addition, their power-up reset feature allows for a user-selectable initial output state of either 0V or midscale and minimizes output voltage glitches during power-up. The serial interface is compatible with SPI(tm), QSPI(tm) and MICROWIRE(tm), which makes the MAX5120/MAX5121 suitable for cascading multiple devices. Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit shift register loads data into the input register. The DAC register may be updated independently or simultaneously with the input register. Both devices are available in a 16-pin QSOP package and are specified for the extended industrial (-40°C to +85°C) temperature range. For pin-compatible 14-bit upgrades, see the MAX5170/MAX5172 data sheet; for pin-compatible 13-bit versions, see the MAX5130/MAX5131 data sheet.

II. Manufacturing Information

A. Description/Function:	+3V/+5V, 12-Bit, Serial, Voltage-Output DACs with Internal Reference
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	January 23, 1999

III. Packaging Information

A. Package Type:	16L QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0499
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	120°C/W
K. Single Layer Theta Jc:	37°C/W
L. Multi Layer Theta Ja:	105°C/W
M. Multi Layer Theta Jc:	37°C/W

IV. Die Information

A. Dimensions:	86 X 144 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.17 @ 25C and 3.00 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DA72 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX5120AEEE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.