MAX5121xEEE
Rev. A

RELIABILITY REPORT

FOR

MAX5121xEEE

PLASTIC ENCAPSULATED DEVICES

February 13, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX5121 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5121 is a low-power, 12-bit, voltage-output digital-to-analog converter (DAC) with an internal precision bandgap reference and an output amplifier. The MAX5121, operating on +3V, delivers its +2.0475V full-scale output with an internal precision reference of +1.25V. If necessary, the user can override the internal, <10ppm/°C voltage reference with an external reference. The device draws only 500µA of supply current, which reduces to 3µA in power-down mode. In addition, the power-up reset feature allows for a user-selectable initial output state of either 0V or midscale and minimizes output voltage glitches during power-up.

The serial interface is compatible with SPI™, QSPI™ and MICROWIRE™, which makes the MAX5121 suitable for cascading multiple devices. This DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit shift register loads data into the input register. The DAC register may be updated independently or simultaneously with the input register.

The device is available in a 16-pin QSOP package and is specified for the extended industrial (-40°C to +85°C) temperature range.

B. Absolute Maximum Ratings

Item	Rating
VDD to AGND,DGND	-0.3V to +6V
AGND to DGND	-0.3V to +0.3V
Digital Inputs to DGND	-0.3V to +6V
Digital Outputs (DOUT, UPO) to DGND	-0.3V to (VDD + 0.3V)
OUT to AGND	-0.3V to (VDD + 0.3V)
OS to AGND	(AGND – 4V) to (VDD + 0.3V)
REF, REFADJ to AGND	-0.3V to (VDD + 0.3V)
Maximum Current into Any Pin	50mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.0mW/°C

II. Manufacturing Information

A. Description: +3V/+5V, 12-Bit, Serial Voltage-Output DAC with Internal Reference

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 3308

D. Fabrication Location: Oregon or California, USA

E. Assembly Location: Thailand

F. Date of Initial Production: January, 1999

III. Packaging Information

A. Package Type: **16-Lead QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0401-0499

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 86 x 144 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 240 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

(4389:) Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 9.99 \times 10^{-9}$ λ = 9.99 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5371) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA72-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX5121xEEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	1
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	740	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package..
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

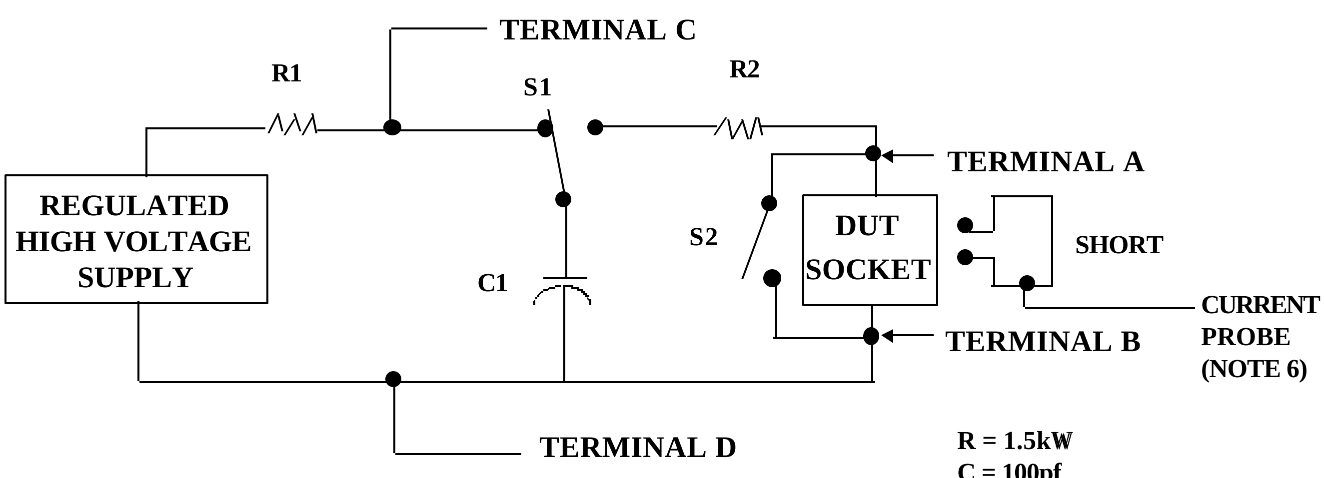
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

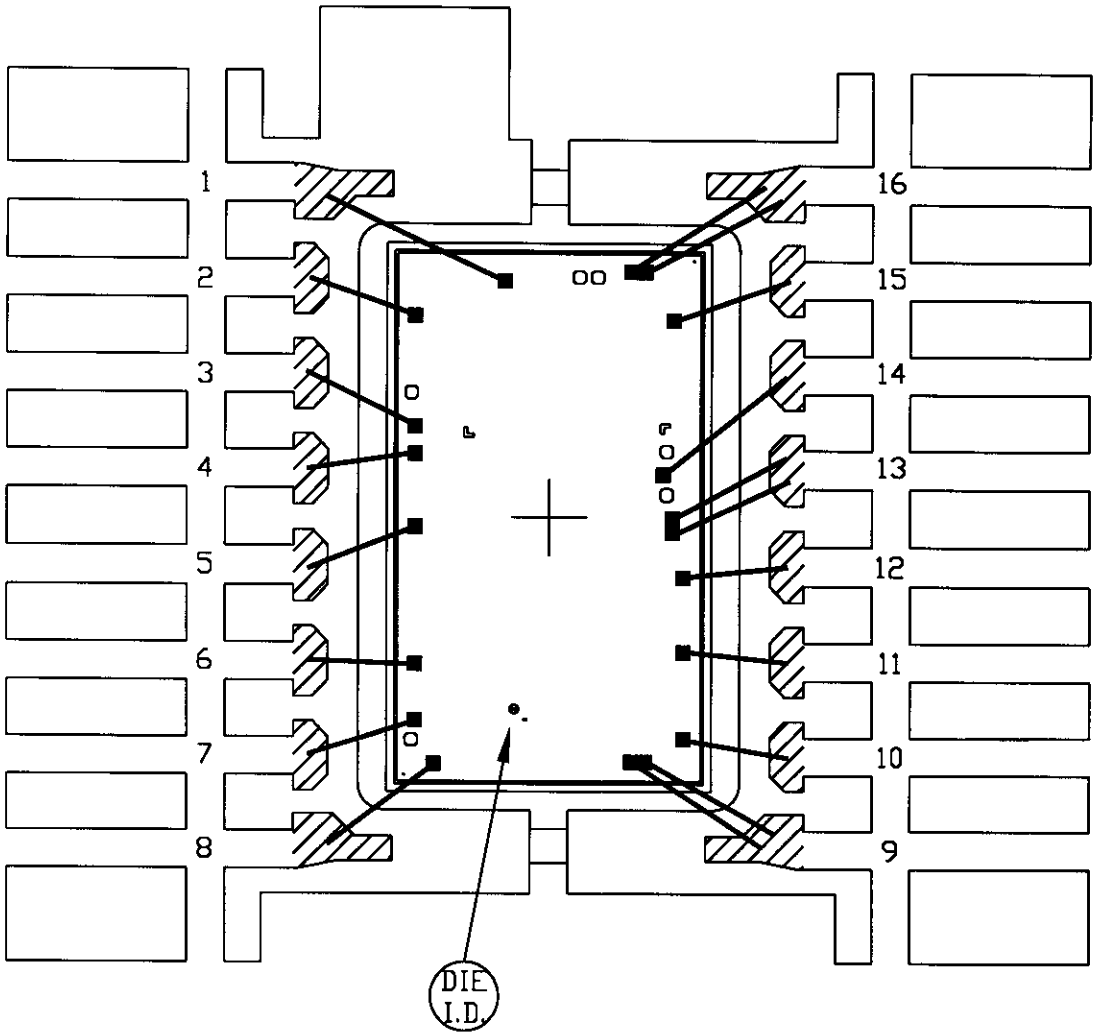
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

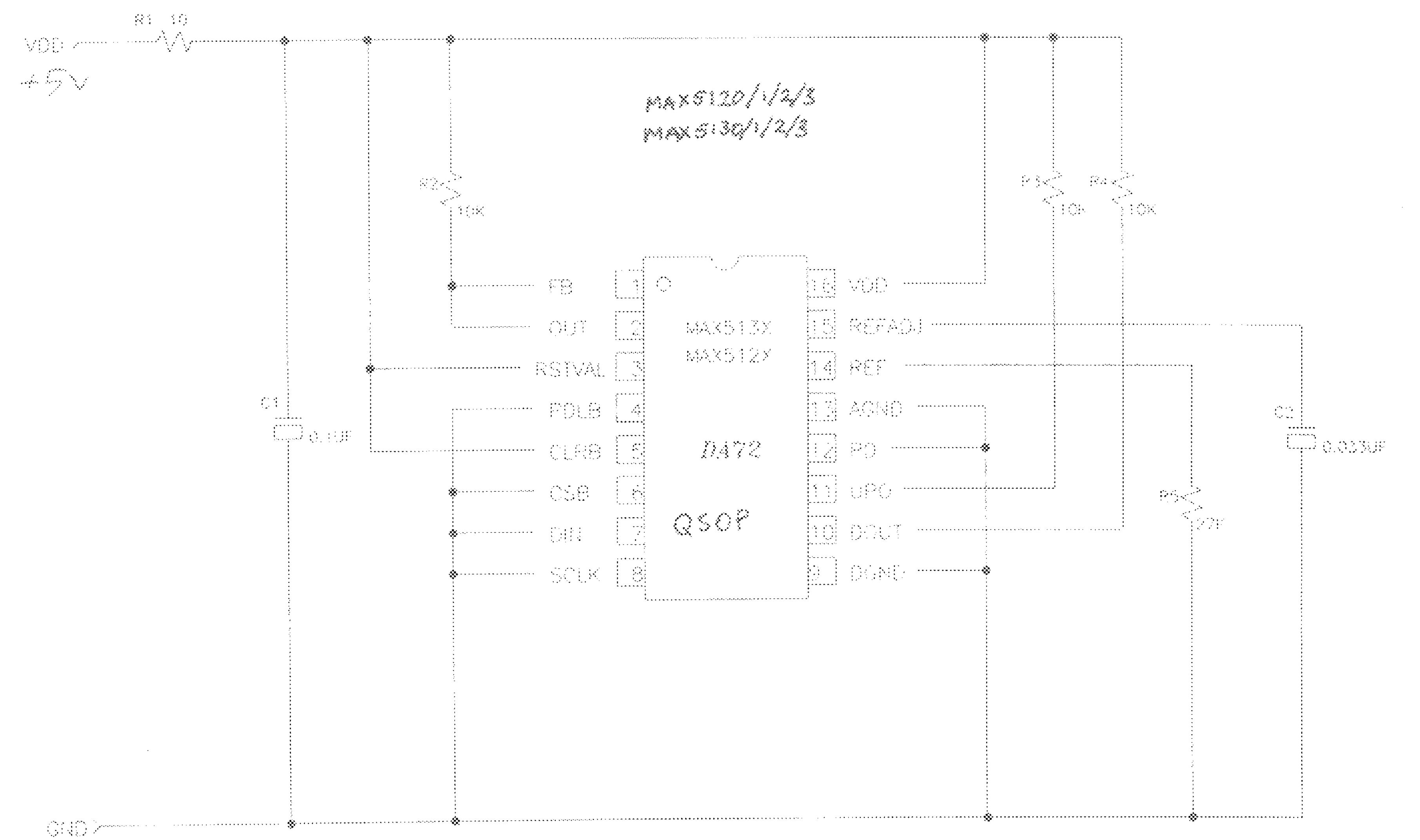
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: E16-5		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 101x154	PKG. DESIGN			BUILDSHEET NUMBER: 05-0401-0499 / REV.: A



Max I_{VDD} : 2.4mA

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