RELIABILITY REPORT

FOR

MAX5138BGTE+T

PLASTIC ENCAPSULATED DEVICES

June 10, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX5138BGTE+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5138/MAX5139 are a family of single-channel pin-compatible and software-compatible 16-bit and 12-bit DACs. The MAX5138/MAX5139 are low-power, 16-bit/12-bit, buffered voltage-output, high-linearity DACs. They use a precision internal reference or a precision external reference for rail-to-rail operation. The MAX5138/MAX5139 accept a wide +2.7V to +5.25V supply-voltage range to accommodate most low-power and low-voltage applications. These devices accept a 3-wire SPI(tm)-/QSPI(tm)-/MICROWIRE(tm)-/DSP-compatible serial interface to save board space and reduce the complexity of optically isolated and transformer-isolated applications. The digital interfaceâ€™s double-buffered hardware and software active-low LDAC provide simultaneous output update. The serial interface features a active-low READY output for easy daisy-chaining of several MAX5138/MAX5139 devices and/or other compatible devices. The MAX5138/MAX5139 include a hardware input to reset the DAC outputs to zero or midscale upon power-up or reset, providing additional safety for applications that drive valves or other transducers that need to be off during power-up. The high linearity of the DACs makes these devices ideal for precision control and instrumentation applications. The MAX5138/MAX5139 are available in an ultra-small (3mm x 3mm), 16-pin TQFN package and are specified over the -40°C to +105°C extended industrial temperature range.

II. Manufacturing Information

A. Description/Function:	Low-Power, Single, 16-/12-Bit, Buffered Voltage-Output DACs
B. Process:	S45
C. Number of Device Transistors:	21088
D. Fabrication Location:	Texas
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 24, 2009

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3491
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	68°C/W
K. Single Layer Theta Jc:	10°C/W
L. Multi Layer Theta Ja:	48°C/W
M. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	71 X 71 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TMRZAQ001A D/C 0837)

The DB44 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX5138BGTE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TMRZAQ001A, D/C 0837

Note 1: Life Test Data may represent plastic DIP qualification lots.