

RELIABILITY REPORT
FOR
MAX519xxxE
PLASTIC ENCAPSULATED DEVICES

April 17, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX519 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX519 is an 8-bit voltage output digital-to-analog converter (DAC) with a simple 2-wire serial interface that allows communication between multiple devices. It operates from a single 5V supply and its internal precision buffer allows the DAC outputs to swing rail-to-rail.

The MAX519 is a dual DACs that uses the supply voltage as the reference for both DACs. The MAX519 features a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, this device can be put into a low-power shutdown mode that reduces supply current to 4 μ A. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V _{DD} to GND	-0.3V to +6V
OUT ₋	-0.3V to (VDD + 0.3V)
AD ₋	-0.3V to (VDD + 0.3V)
SCL, SDA to GND	-0.3V to +6V
Maximum Current into Any Pin	50mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin NSO	696mW
16-Pin PDIP	842mW
Derates above +70°C	
16-Pin NSO	8.70mW/°C
16-Pin PDIP	10.53mW/°C

II. Manufacturing Information

A. Description/Function:	2-Wire Serial 8-Bit DACs with Rail-to-Rail Outputs
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	1797
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	June, 1995

III. Packaging Information

A. Package Type:	16-Lead NSO	16-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0401-0433	# 05-0401-0432
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

IV. Die Information

A. Dimensions:	78 x 135 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 480 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 2.26 \times 10^{-9} \quad \lambda = 2.26 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5122) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA53-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX519xxxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		480	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

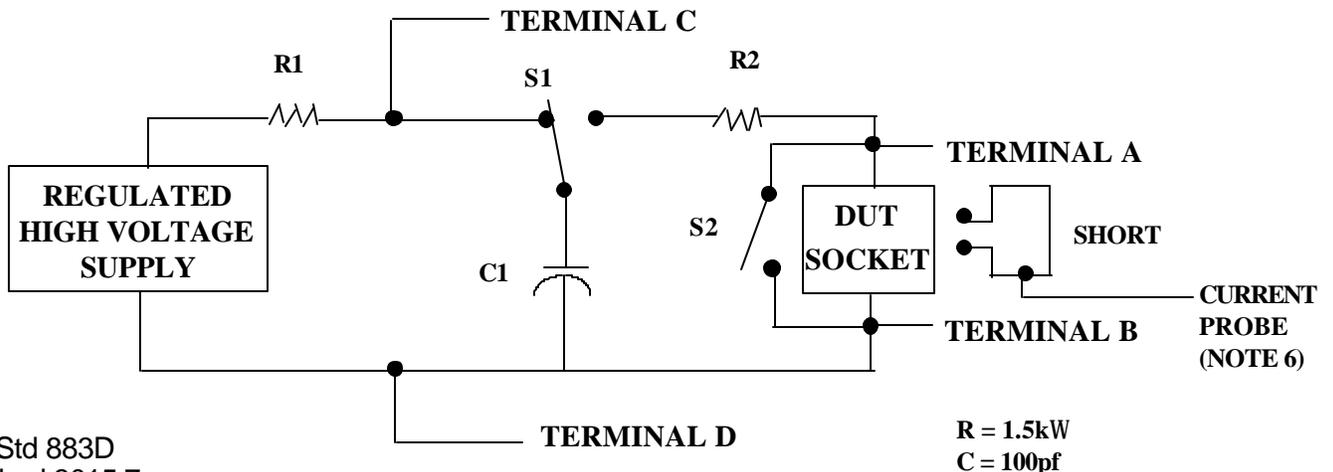
2/ No connects are not to be tested.

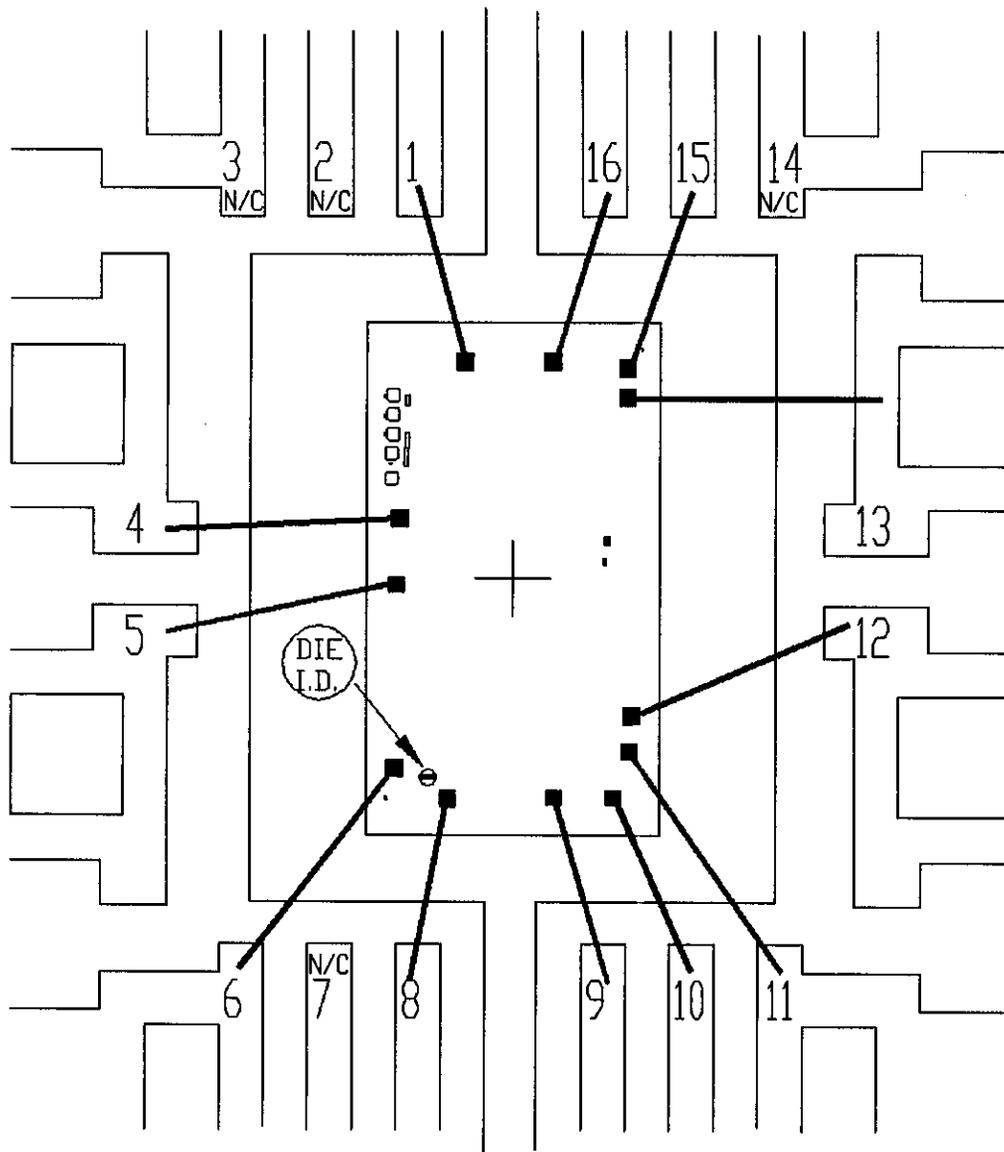
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: P16-2

CAV./PAD SIZE: 140 x 170

PKG.
DESIGN

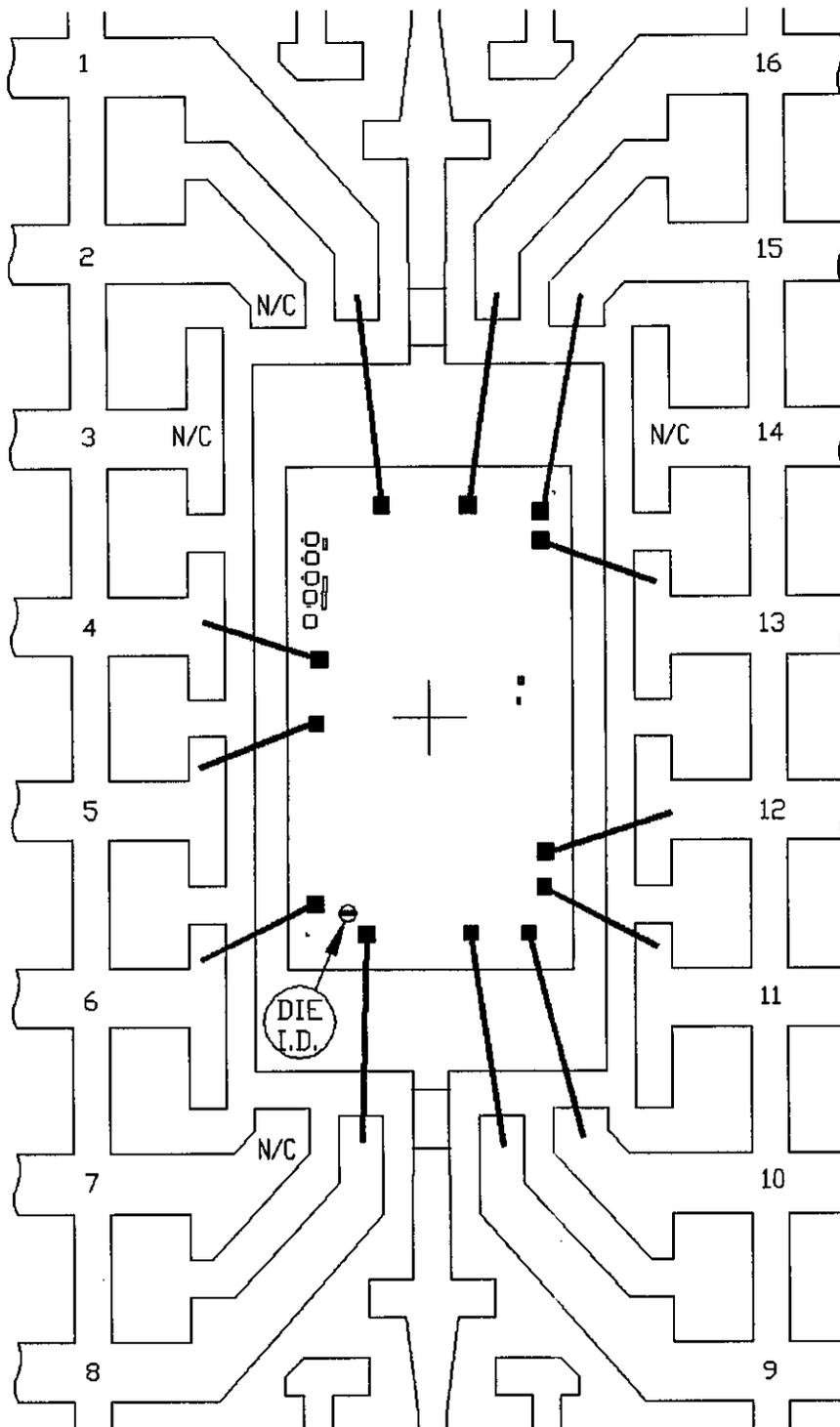
APPROVALS

DATE

MAXIM

BUILDSHEET NUMBER:
05-0401-0432

REV.:
A



PKG.CODE: S16-5

CAV./PAD SIZE:
96X190

PKG.
DESIGN

APPROVALS

DATE

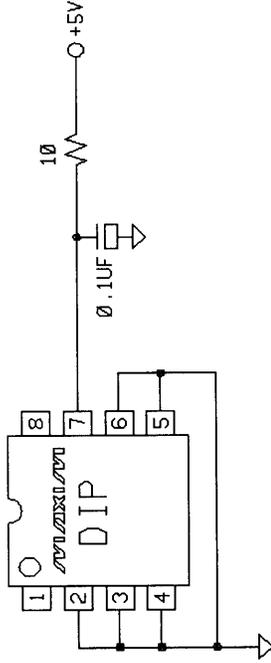
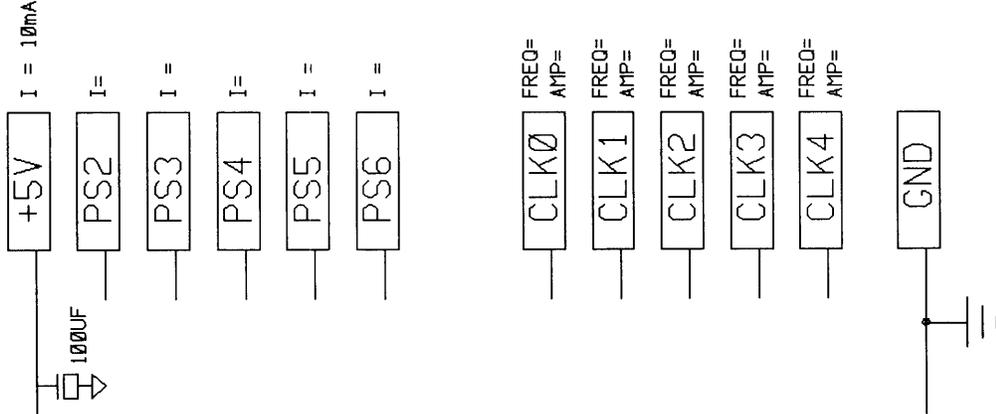
MAXIM

BUILD SHEET NUMBER:
05-0401-0433

REV.:
A

ONCE PER BOARD

ONCE PER DEVICE



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 - BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES :

1. TEMPERATURE : 125C OR EQUIVALENT
2. TIME : 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

SPEC. NO. 06-5122 REV : A

MAXIM BURN-IN SCHEMATIC

DATE : 4/12/95

DEVICE TYPE(S) :

MAX517/518

DRAWN BY :