MAX5403EUB
Rev. A

RELIABILITY REPORT

FOR

MAX5403EUB

PLASTIC ENCAPSULATED DEVICES

May 11, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX5403 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5403 is a dual linear taper digital potentiometer. Thus device has one 3-terminal potentiometer and one 2-terminal variable resistor (Figure 1). The MAX5403 operates from +2.7V to +5.5V single supply voltages and use an ultra-low supply current of 0.1µA. This device also provide glitchless switching between resistors taps as well as a convenient power-on reset (POR) that sets the wiper to the midscale position at power-up. The potentiometer consists of a fixed resistor with a wiper contact that is digitally controlled through a 3-wire serial interface and has 256 tap points. It performs the same function as a discrete potentiometer or variable resistor.

These parts are ideal for applications requiring digitally controlled resistors. The device has a resistance values of10kΩ. A nominal resistor temperature coefficient of 35ppm/°C end-to-end and 5ppm/°C ratiometric make the MAX5403 ideal for applications requiring low temperature-coefficient variable resistors, such as adjustable-gain circuit configurations.

The MAX5403 is available in a 10-pin µMAX package. The device is guaranteed over the extended industrial temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
DIN, SCLK, CS	-0.3V to +6V
HX, LX, WX to GND	-0.3V to (VDD + 0.3)
Maximum Continuous Current Into HX, LX, and WX	±1mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin µMAX	444mW
Derates above +70°C	
10-Pin µMAX	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	Dual 256-Tap, Low-Drift, Digital Potentiometers
B. Process:	S6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	8689
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**10-Pin µMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-7001-0487
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	75 x 88 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$

$\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5690) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DP03 die type has been found to have all pins able to withstand a transient pulse of ±1500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX5403EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

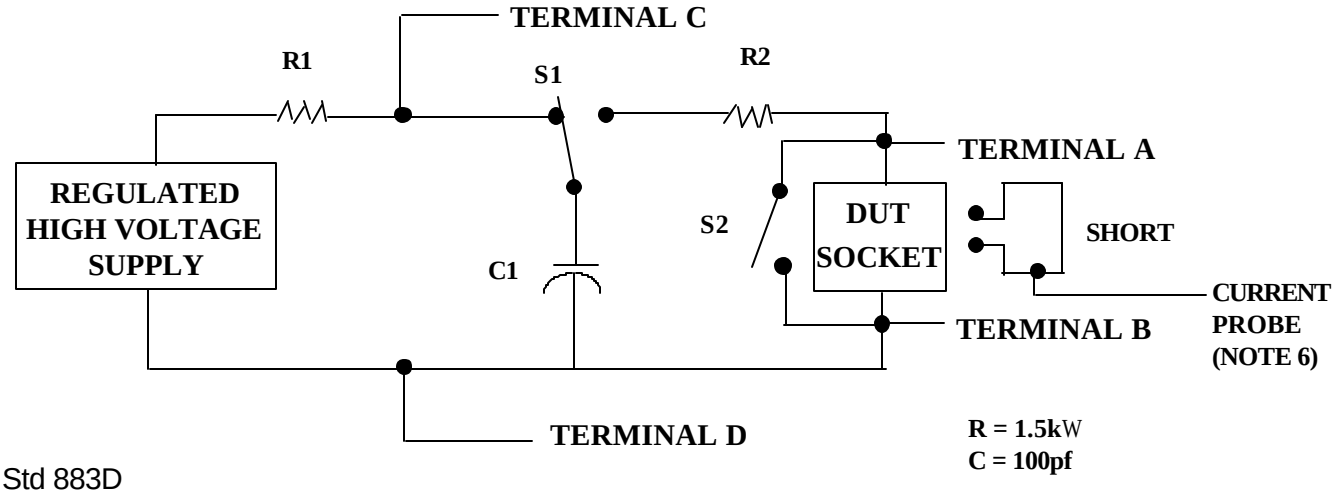
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

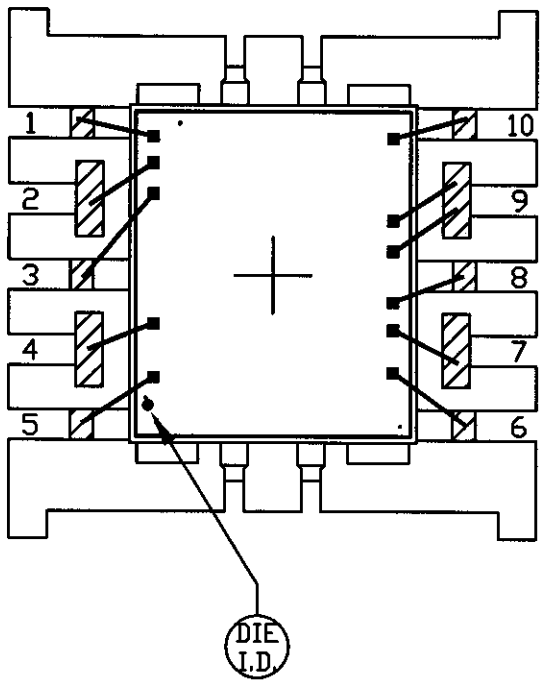
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

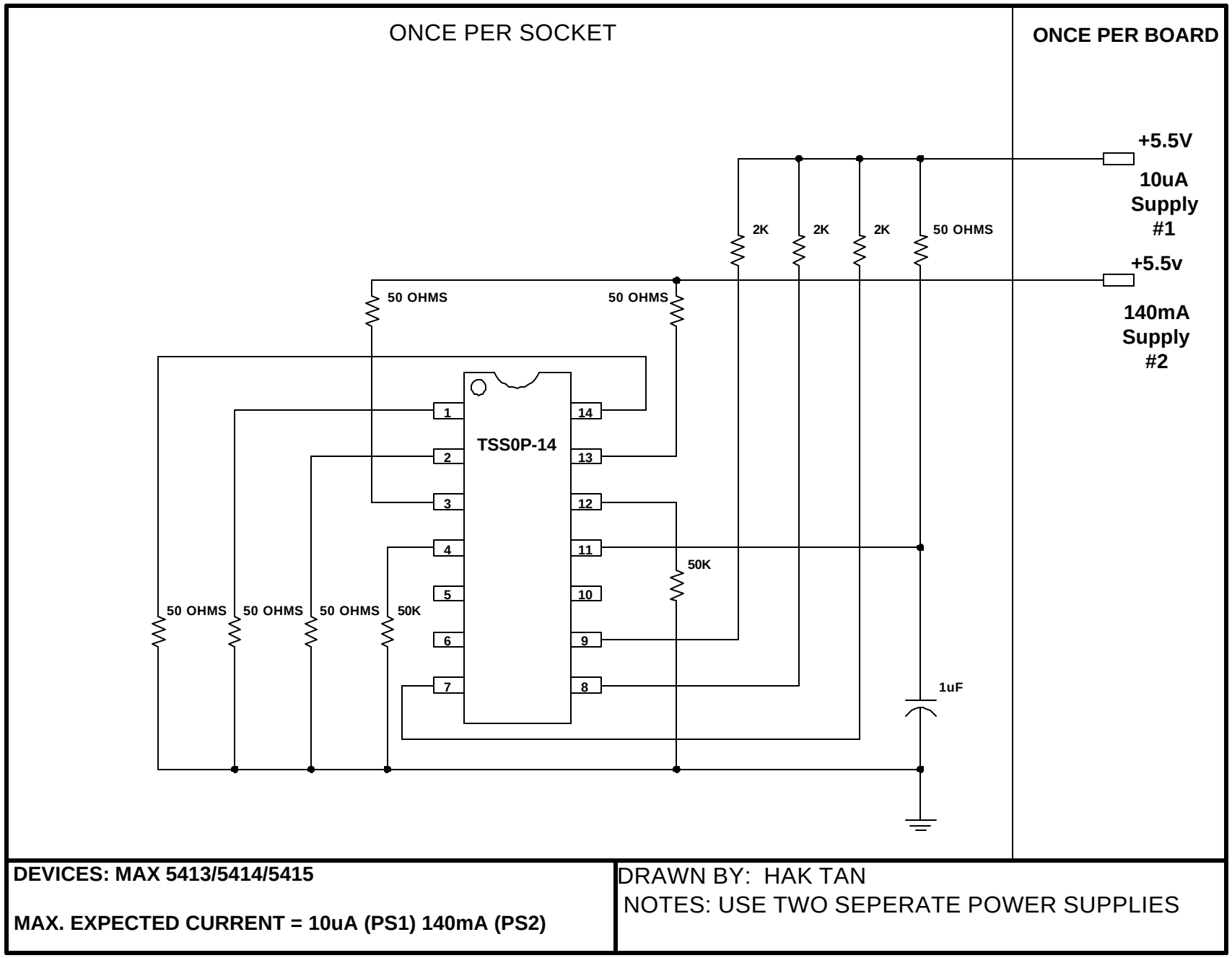


Mil Std 883D
Method 3015.7
Notice 8



BONDING AREA

PKG. CODE: U10C-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: CHIP ON LEAD	PKG. DESIGN			BOND DIAGRAM #: 05-7001-0487 / REV: A



DEVICES: MAX 5413/5414/5415

MAX. EXPECTED CURRENT = 10uA (PS1) 140mA (PS2)

DRAWN BY: HAK TAN

NOTES: USE TWO SEPERATE POWER SUPPLIES