RELIABILITY REPORT

FOR

MAX5419META+T

PLASTIC ENCAPSULATED DEVICES

February 4, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The MAX5419META+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5417/MAX5418/MAX5419 nonvolatile, linear-taper, digital potentiometers perform the function of a mechanical potentiometer by replacing the mechanics with a simple 2-wire digital interface, allowing communication with multiple devices. Each device performs the same function as a discrete potentiometer or variable resistor and has 256 tap points. The devices feature an internal, nonvolatile EEPROM used to store the wiper position for initialization during power-up. The fast-mode I^{2}C-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnection complexity in many applications. Each device is available with one of four factory-preset addresses (see the *Ordering Information/Selector Guide* in the full data sheet) and features an address input for a total of eight unique address combinations. The MAX5417/MAX5418/MAX5419 provide three nominal resistance values: 50k (MAX5417), 100k (MAX5418), or 200k (MAX5419). The nominal resistor temperature coefficient is 35ppm/°C end-to-end, and only 5ppm/°C ratiometric. This makes the devices ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain-amplifier circuit configurations. The MAX5417/MAX5418/MAX5419 are available in a 3mm x 3mm 8-pin TDFN package, and are specified over the extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers
B. Process:	E35
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	July 24, 2004

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3154
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.3°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.3°C/W

IV. Die Information

A. Dimensions:	61X45 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35um
F. Minimum Metal Spacing:	0.35um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 288 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.82 \times 10^{-9}$

λ = 3.82 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the E35 Process results in a FIT Rate of 2.66 @ 25C and 46.05 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot CNS2CA007A D/C 0531, Latch-Up lot CNSXBA008A D/C 0510)

The DP16-5 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1

Reliability Evaluation Test Results

MAX5419META+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	DNS0EQ003C, D/C 0823
	Biased	& functionality	48	0	DNS8DA009G, D/C 0841
	Time = 192 hrs.		48	0	DNS4DA004D, D/C 0816
			48	0	CNS1CA011A, D/C 0614
			48	0	CNSXBA008A, D/C 0510
			48	0	CNS0AQ001A, D/C 0401

Note 1: Life Test Data may represent plastic DIP qualification lots.

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