RELIABILITY REPORT

FOR

MAX542xxxD

PLASTIC ENCAPSULATED DEVICES

June 14, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX542 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX542 is a serial-input, voltage-output, 16-bit digital-to-analog converter (DAC) that operates from a single +5V supply. It provides 16-bit performance (±1LSB INL and DNL) over temperature without any adjustments. The DAC output is unbuffered, resulting in a low supply current of 0.3mA and a low offset error of 1LSB.

The DAC output range is 0V to V_{REF}. A 16-bit serial word is used to load data into the DAC latch. The 6.25MHz, 3-wire serial interface is compatible with SPI™/QSPI™/Microwire™, and it also interfaces directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the DAC output to 0V (unipolar mode) when power is initially applied.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to DGND	-0.3V to +6V
/CS, SCLK, DIN, /LDAC to DGND	-0.3V to +6V
REF, REFF, REFS to AGND_	-0.3V to V_{DD} +0.3V
AGND, AGNDF, AGNDS to DGND	-0.3V to +0.3V
OUT, INV to AGND_, DGND	-0.3V to V_{DD}
RFB to AGND_, DGND	-6V to +6V
Maximum Current into Any Pin	50mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
14-Pin PDIP	800mW
14-Pin SO	667mW
Derates above +70°C	
14-Pin PDIP	10.0mW/°C
14-Pin SO	8.33mW/°C

II. Manufacturing Information

A. Description/Function:	+5V, Serial-Input, Voltage-Output, 16-Bit DAC
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	2209
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	December, 1996

III. Packaging Information

A. Package Type:	8 Lead PDIP	8-Lead SO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0401-0496	Buildsheet # 05-0401-0497
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	85 x 139 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 303 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 3.58 \times 10^{-9}$

$\lambda = 3.58$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5181) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DA58 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results
MAX542xxxD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		303	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	PDIP SO	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic/Package process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

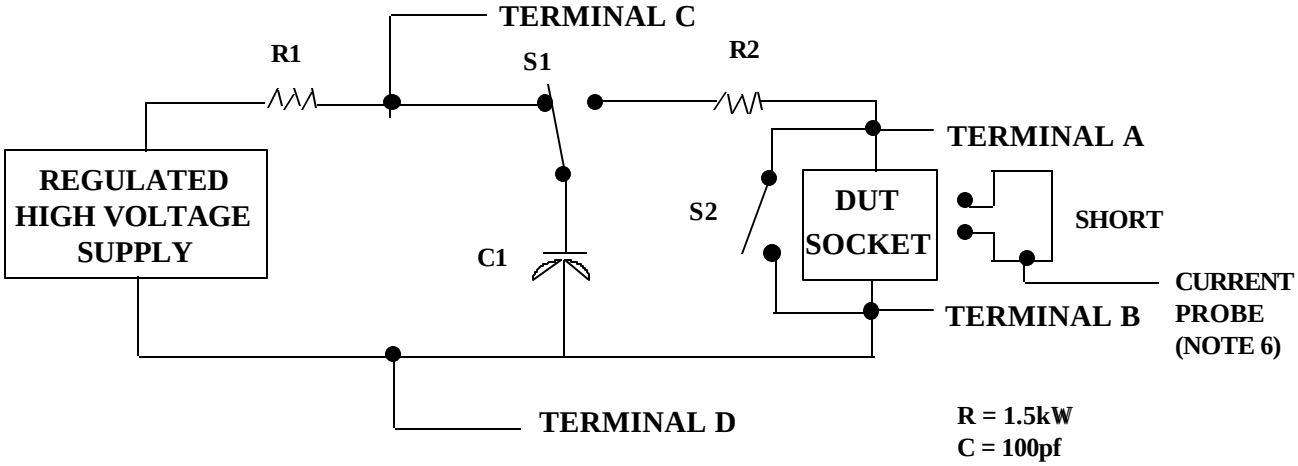
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

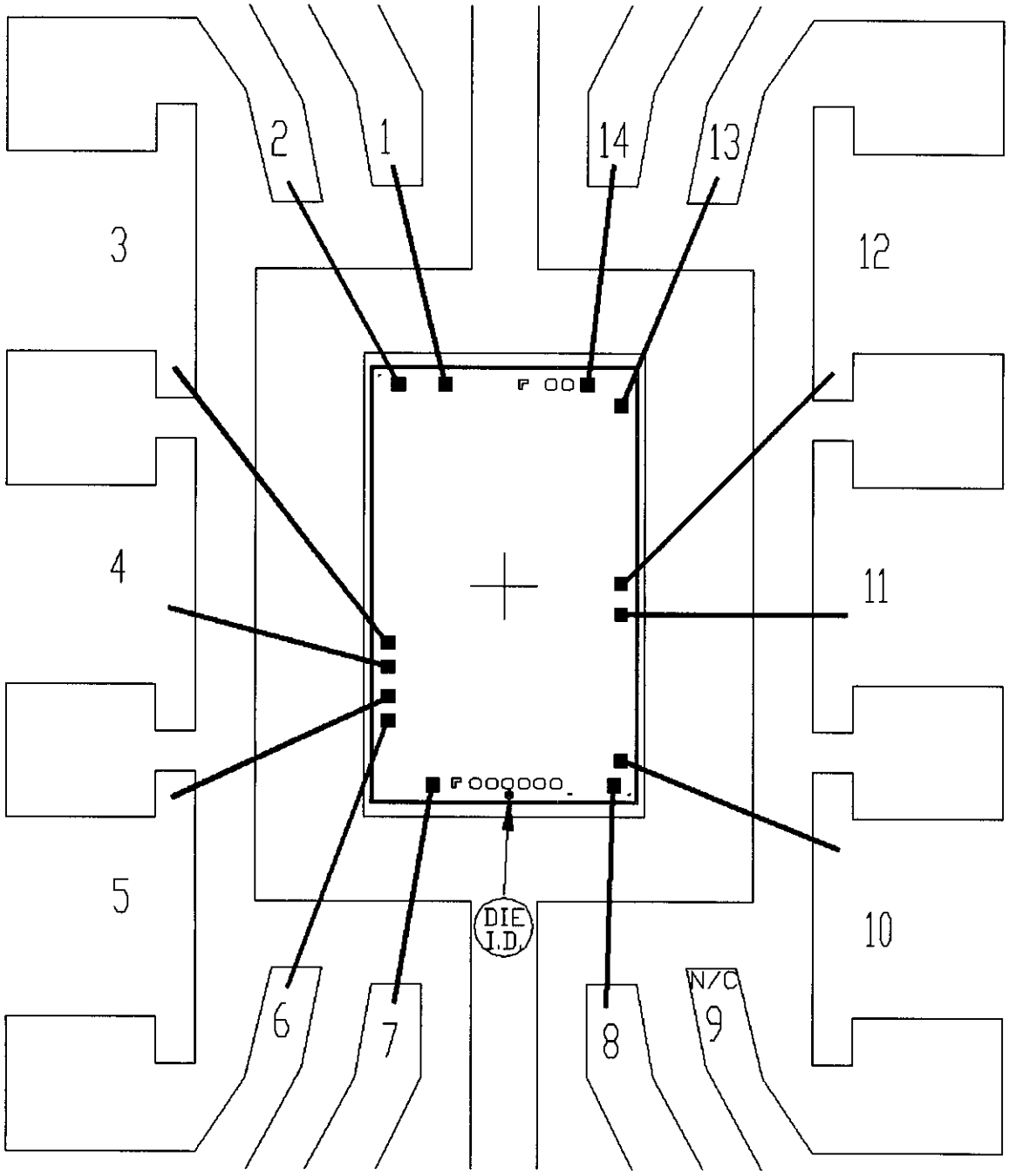
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

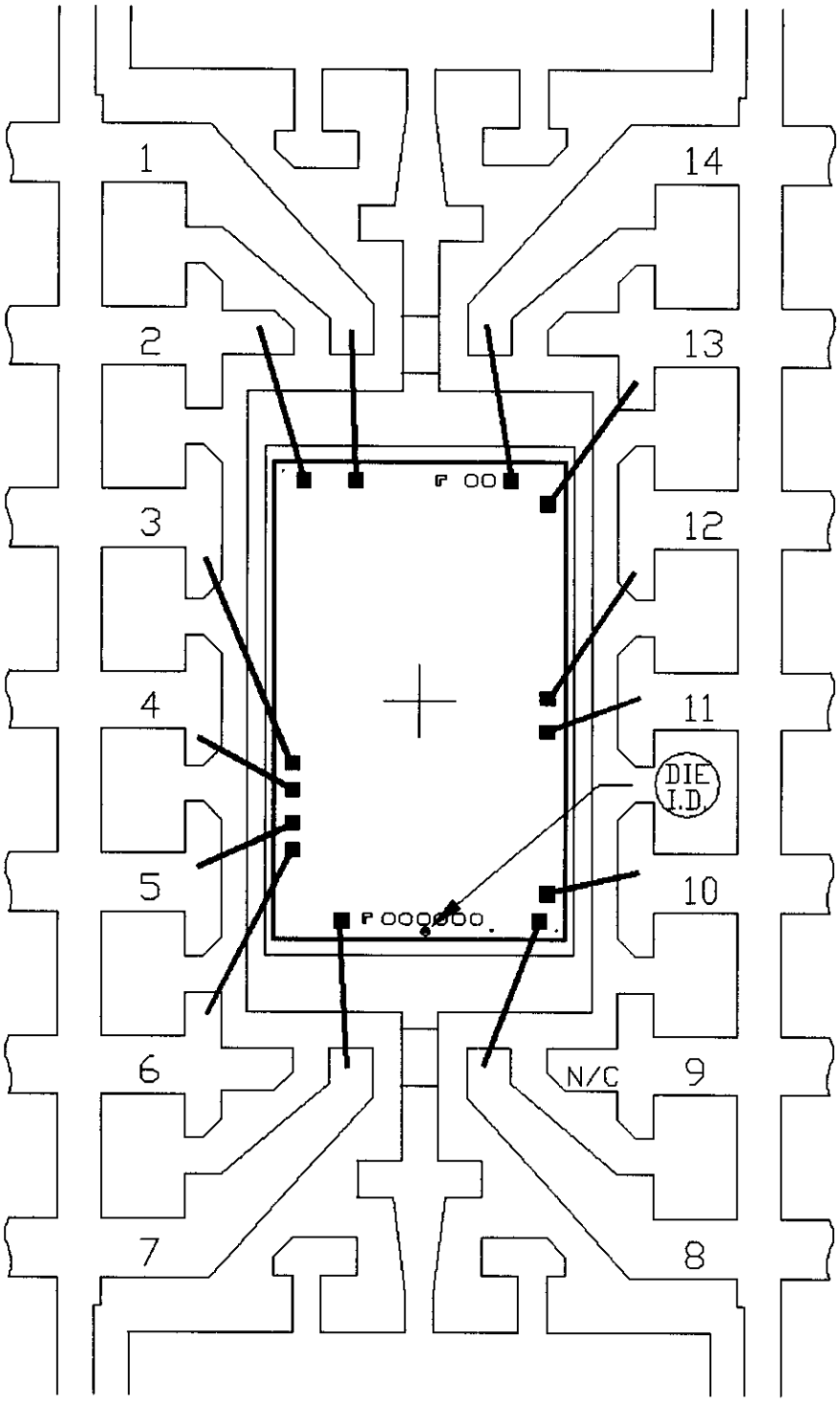
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

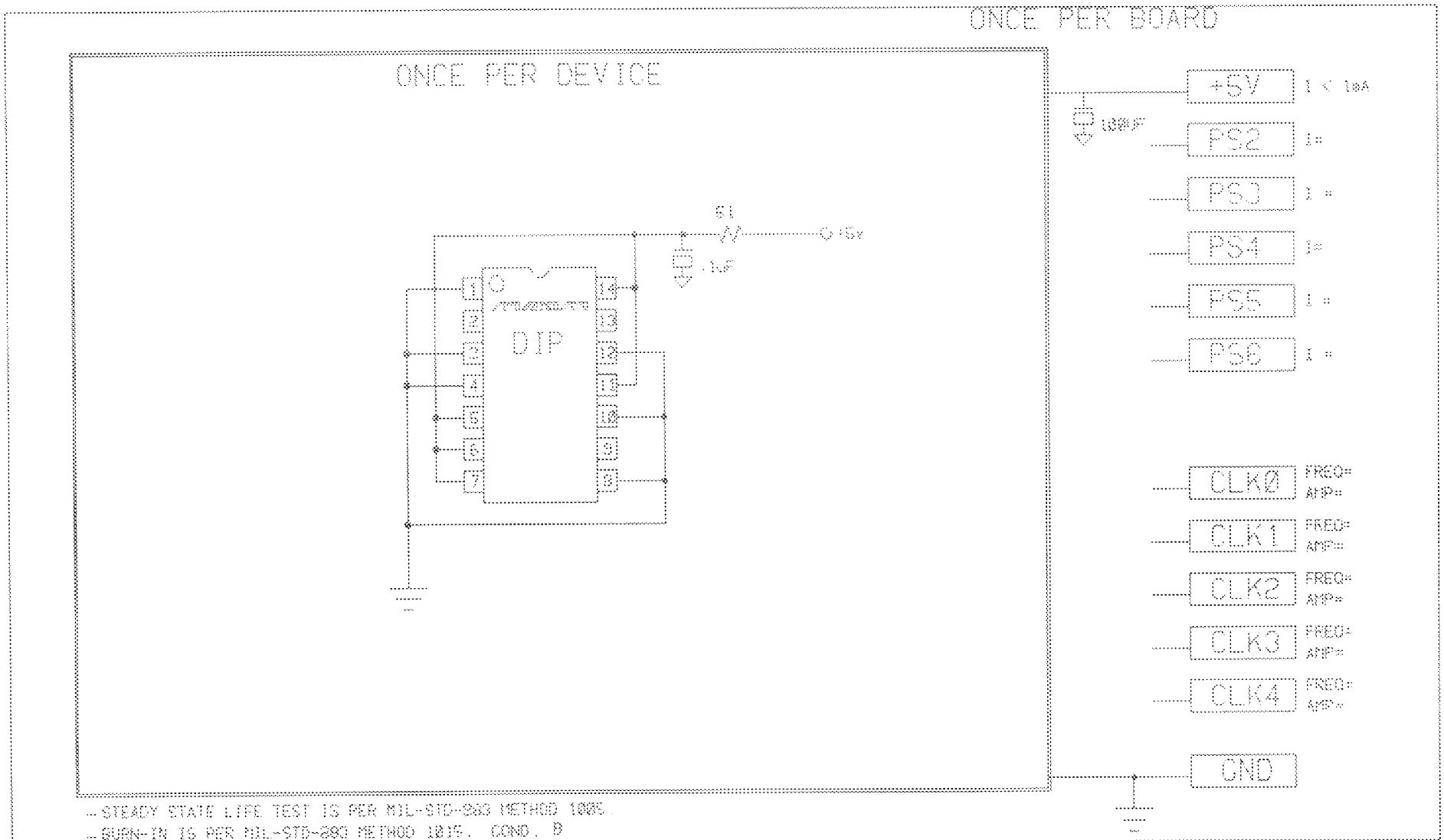




PKG.CODE: P14-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 150 X 190	PKG. DESIGN			BUILDSHEET NUMBER: 05-0401-0496 REV.: A



PKG.CODE: S14-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 95X170	PKG. DESIGN			BUILDSHEET NUMBER: 05-0401-0497 / REV.: A



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. D

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MIL/883

SPEC. NO. 06-5191 REV: A

DATE: 2/06/96

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX544/545