RELIABILITY REPORT

FOR

MAX5420xUA

PLASTIC ENCAPSULATED DEVICES

November 15, 2005

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX5420 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

The MAX5420 is a digitally programmable precision voltage divider optimized for use in digitally programmable gain amplifier configurations. The MAX5420 operates from a single +5V supply or dual ±5V supply, and consumes only 3µA supply current. This device consists of a digitally selectable resistor array that provides four precision noninverting gains of 1, 2, 4, and 8 for PGAs. The MAX5420 achieves a resistor ratio accuracy of 0.025% (MAX5420A), 0.09% (MAX5420B), and 0.5% (MAX5420C).

The MAX5420 is available in a 8-pin µMAX package. The device is specified over the extended temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
VSS to GND	+0.3V to -6V
D0, D1 to GND	-0.3V to (VDD + 0.3V)
H, L, W, MATCH_ to GND	(VSS - 0.3V) to (VDD + 0.3V)
Input and Output Latchup Immunity	±50mA
Continuous Power Dissipation (TA = +70°C)	
8-Pin µMAX (derate 4.1mW/°C above +70°C)	333mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Digitally Programmable Precision Voltage Divider for PGAs
B. Process:	S3
C. Number of Device Transistors:	118
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	October, 2001

III. Packaging Information

A. Package Type:	**8-Pin µMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3401-0013
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	62 x 70 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.74 \times 10^{-9}$ $\lambda = 13.74$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5741) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.23 @ 25C and 3.95 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DP08 die type has been found to have all pins able to withstand a transient pulse of +/-1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

Table 1
Reliability Evaluation Test Results

MAX5420xUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT TDFN	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

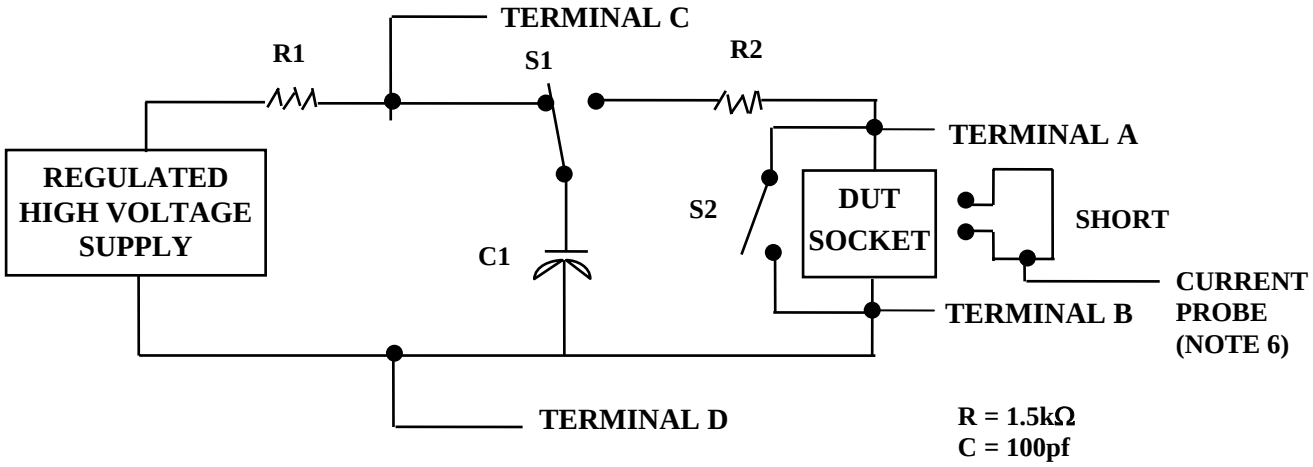
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

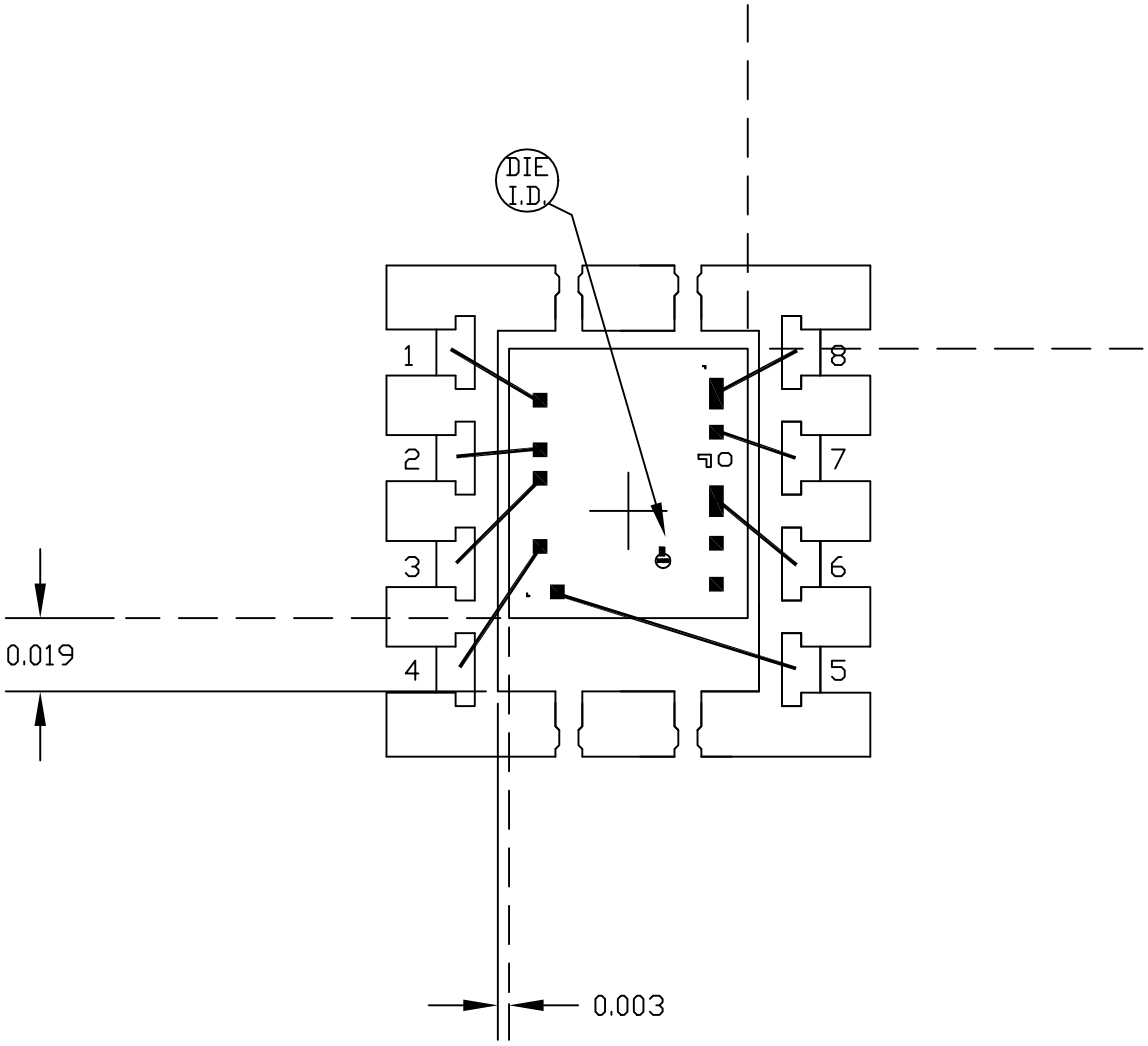
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

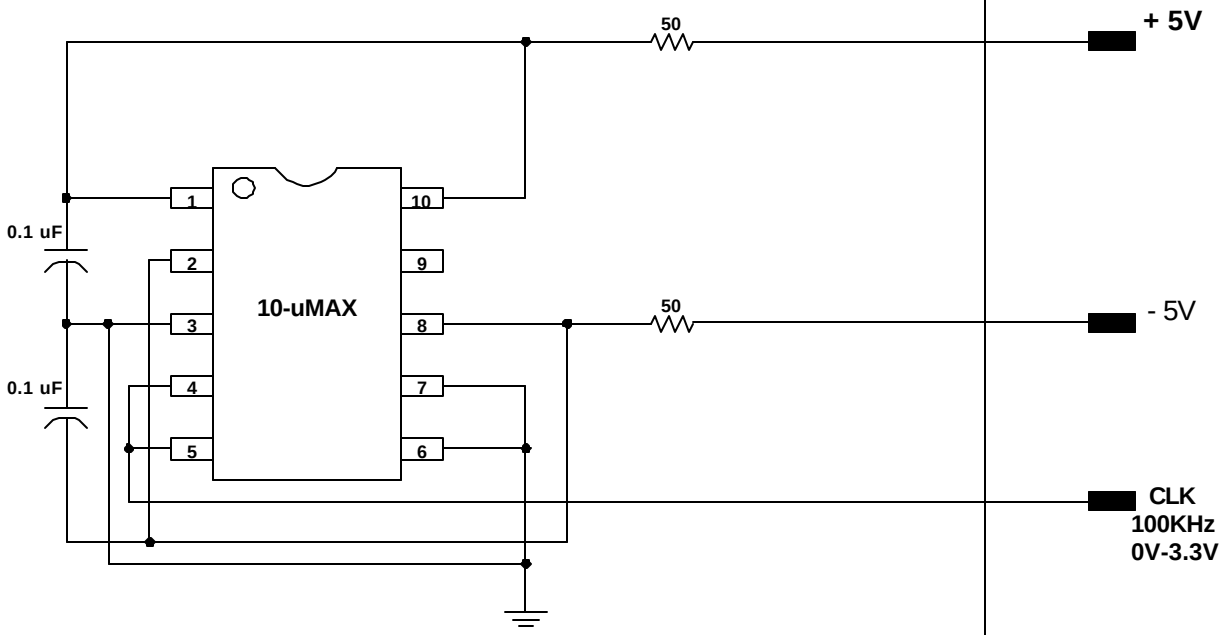




PKG. CODE: U8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.	RAMON DE LEON	6/27/01	BOND DIAGRAM #: 05-3401-0013	REV: C
	DESIGN	YINGYING WEI	6/27/01		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 5421A/5421B/5421C

MAX. EXPECTED CURRENT = 50mA

NOTES: