RELIABILITY REPORT

FOR

MAX5488ETE+T

PLASTIC ENCAPSULATED DEVICES

July 2, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering

Conclusion

The MAX5488ETE+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5487/MAX5488/MAX5489 dual, linear-taper, digital potentiometers function as mechanical potentiometers with a simple 3-wire SPI(tm)-compatible digital interface that programs the wipers to any one of 256 tap positions. These digital potentiometers feature a nonvolatile memory (EEPROM) to return the wipers to their previously stored positions upon power-up. The MAX5487 has an end-to-end resistance of 10kΩ, while the MAX5488 and MAX5489 have resistances of 50kΩ and 100kΩ, respectively. These devices have a low 35ppm/°C end-to-end temperature coefficient, and operate from a single +2.7V to +5.25V supply. The MAX5487/MAX5488/MAX5489 are available in 16-pin 3mm x 3mm x 0.8mm thin TQFN or 14-pin TSSOP packages. Each device is guaranteed over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Dual, 256-Tap, Nonvolatile, SPI-Interface, Linear-Taper Digital Potentiometers	
B. Process:	E35	
C. Fabrication Location:	USA	
D. Assembly Location:	Japan, Thailand	Malaysia, Philippines, Thailand
E. Date of Initial Production:	October 23, 2004	

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3	14-pin TSSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	N/A (N/A mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1182	#05-9000-1181
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	N/A°C/W	110°C/W
K. Single Layer Theta Jc:	N/A°C/W	30°C/W
L. Multi Layer Theta Ja:	57.2°C/W	100.4°C/W
M. Multi Layer Theta Jc:	40°C/W	30°C/W

IV. Die Information

A. Dimensions:	91X94 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 microns (as drawn)
F. Minimum Metal Spacing:	0.35 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 144 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.6 \times 10^{-9}$

$\lambda = 7.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the E35 Process results in a FIT Rate of 0.68 @ 25°C and 11.68 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The DP21-1 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5488ETE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125°C Biased Time = 192 hrs.	DC Parameters & functionality	144	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.