

RELIABILITY REPORT  
FOR  
MAX5489ETE+  
PLASTIC ENCAPSULATED DEVICES

January 28, 2011

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

<b>Approved by</b>
Sokhom Chum
Quality Assurance
Reliability Engineer

## Conclusion

The MAX5489ETE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

<b>I. ....Device Description</b>	<b>V. ....Quality Assurance Information</b>
<b>II. ....Manufacturing Information</b>	<b>VI. ....Reliability Evaluation</b>
<b>III. ....Packaging Information</b>	<b>IV. ....Die Information</b>
<b>.....Attachments</b>	

### I. Device Description

#### A. General

The MAX5487/MAX5488/MAX5489 dual, linear-taper, digital potentiometers function as mechanical potentiometers with a simple 3-wire SPI(tm)-compatible digital interface that programs the wipers to any one of 256 tap positions. These digital potentiometers feature a nonvolatile memory (EEPROM) to return the wipers to their previously stored positions upon power-up. The MAX5487 has an end-to-end resistance of 10k , while the MAX5488 and MAX5489 have resistances of 50k and 100k , respectively. These devices have a low 35ppm/°C end-to-end temperature coefficient, and operate from a single +2.7V to +5.25V supply. The MAX5487/MAX5488/MAX5489 are available in 16-pin 3mm x 3mm x 0.8mm thin QFN or 14-pin TSSOP packages. Each device is guaranteed over the extended -40°C to +85°C temperature range.

## II. Manufacturing Information

A. Description/Function:	Dual, 256-Tap, Nonvolatile, SPI-Interface, Linear-Taper Digital Potentiometers
B. Process:	E35
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	January 22, 2005

## III. Packaging Information

A. Package Type:	16-pin TQFN 3x3 FLIP CHIP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	None
E. Bondwire:	0.005HL
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1182
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	57.2°C/W
M. Multi Layer Theta Jc:	40°C/W

## IV. Die Information

A. Dimensions:	91 X 94 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 125°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 192 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 5.7 \times 10^{-9}$$
$$\lambda = 5.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the E35 Process results in a FIT Rate of 0.68 @ 25C and 11.68 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot CSE2AQ002 D/C 0438)

The DP21-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX5489ETE+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C	DC Parameters	48	0	DSE0BQ001A, D/C 0547
	Biased	& functionality	48	0	DSE0CA001C, D/C 0640
	Time = 192 hrs.		48	0	DSE0D3046A, D/C 0906
				48	0

Note 1: Life Test Data may represent plastic DIP qualification lots.