RELIABILITY REPORT

FOR

MAX5715AAUD+ / MAX5715AWC+T

PLASTIC ENCAPSULATED DEVICES /
WAFER LEVEL PRODUCTS

July 19, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX5715AAUD+ / MAX5715AWC+Tsuccessfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5713/MAX5714/MAX5715 4-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5713/MAX5714/MAX5715 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (3mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100k (typ) load to an external reference. The MAX5713/MAX5714/MAX5715 have a 50MHz 3-wire SPI/QSPI(tm) /MICROWIRE®/DSP-compatible serial interface that also includes an active-low RDY output for daisy-chain applications. The DAC output is buffered and has a low supply current of less than 250µA per channel and a low offset error of ±0.5mV (typ). On power-up, the MAX5713/MAX5714/MAX5715 reset the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference. The MAX5713/MAX5714/MAX5715 allow simultaneous output updates using software LOAD commands or the hardware load DAC logic input (active-low LDAC). A clear logic input (active-low CLR) allows the contents of the CODE and the DAC registers to be cleared asynchronously and sets the DAC outputs to zero. The MAX5713/MAX5714/MAX5715 are available in a 14-pin TSSOP and an ultra-small, 12-bump WLP package and are specified over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface	
B. Process:	S18	
C. Number of Device Transistors:	43896	
D. Fabrication Location:	USA	
E. Assembly Location:	Malaysia, Philippines and Thailand	Japan
F. Date of Initial Production:	June 29, 2012	

III. Packaging Information

A. Package Type:	14-pin TSSOP	12-bump WLP 3x4 array
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-4971	#05-9000-4954
H. Flammability Rating:	Class UL94-V0	
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	110°C/W	°C/W
K. Single Layer Theta Jc:	30°C/W	°C/W
L. Multi Layer Theta Ja:	100.4°C/W	62°C/W
M. Multi Layer Theta Jc:	30°C/W	°C/W

IV. Die Information

A. Dimensions:	60.2362X80.3149 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAGO4Q001G, D/C 1219)

The DB51-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5715AAUD+/ MAX5715AWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	SAGO4Q001H, D/C 1219

Note 1: Life Test Data may represent plastic DIP qualification lots.