

RELIABILITY REPORT  
FOR  
MAX5723AUP+T  
PLASTIC ENCAPSULATED DEVICES

May 26, 2013

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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## Conclusion

The MAX5723AUP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX5723/MAX5724/MAX5725 8-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal 3ppm/°C reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5723/MAX5724/MAX5725 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (6mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100k (typ) load to an external reference. The MAX5723/MAX5724/MAX5725 have a fast 50MHz, 4-wire SPI/QSPI(tm)/MICROWIRE®/DSP-compatible serial interface that operates at clock rates up to 50MHz. The DAC output is buffered and has a low supply current of less than 250µA per channel and a low offset error of ±0.5mV (typ). On power-up, the MAX5723/MAX5724/MAX5725 reset the DAC outputs to zero or midscale based on the status of M/active-low Z logic input, providing flexibility for a variety of control applications. The internal reference is initially powered down to allow use of an external reference. The MAX5723/MAX5724/MAX5725 allow simultaneous output updates using software LOAD commands or the hardware load DAC logic input (active-low LDAC). The MAX5723/MAX5724/MAX5725 feature a programmable watchdog function which can be enabled to monitor the I/O interface for activity and integrity. A clear logic input (active-low CLR) allows the contents of the CODE and the DAC registers to be cleared asynchronously and simultaneously sets the DAC outputs to the programmable default value. The MAX5723/MAX5724/MAX5725 are available in a 20-pin TSSOP and an ultra-small, 20-bump WLP package and are specified over the -40°C to +125°C temperature range.

## II. Manufacturing Information

A. Description/Function:	Ultra-Small, Octal-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface
B. Process:	S18
C. Number of Device Transistors:	89328
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	March 29, 2013

## III. Packaging Information

A. Package Type:	20-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4587
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	91°C/W
K. Single Layer Theta Jc:	20°C/W
L. Multi Layer Theta Ja:	73.8°C/W
M. Multi Layer Theta Jc:	20°C/W

## IV. Die Information

A. Dimensions:	100 X 90.1575 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 6.9 \times 10^{-9}$$

$$\lambda = 6.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot SACJ9Q002A, D/C 1213)

The DB48 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX5723AUP+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C	DC Parameters	80	0	SACJ9Q002A, D/C 1213
	Biased	& functionality	80	0	SACJ9Q001C, D/C 1146
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.