RELIABILITY REPORT

FOR

MAX5862AUXH+ / MAX5862BUXH+ /
MAX5862CUXH+ / MAX5862DUXH+

WAFER LEVEL DEVICES

June 23, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering

Conclusion

The MAX5862AUXH+ / MAX5862BUXH+ / MAX5862CUXH+ / MAX5862DUXH+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX5862 is an integrated, high-density, downstream cable QAM modulator, digital upconverter (DUC) and RF digital-to-analog converter (RF-DAC). The device performs QAM mapping, pulse shaping and digital RF upconversion of forward-error-correction (FEC) encoded data with full agility and drives a single RF-port using a 14-bit 4.6Gsps DAC. The device digitally synthesizes RF signals with up to 32 DOCSIS-compliant 6MHz QAM or 8MHz QAM channels. The device has fixed QAM capacity and provides high-density QAM modulation with very low power dissipation (4.2W at 32 QAMs) in a compact 12mm x 17mm footprint. The device accepts FEC-encoded CMOS data (symbols) on a single 10-bit input port that accepts up to 32 time-interleaved digital data streams. Each channel features an individually configurable QAM mapper, RRC filter, and arbitrary rate resampler (ARR). The device performs pulse shaping, resampling, interpolation and quadrature modulation of input data, supporting all data rates defined in DOCSIS 3.0 and DVB-C. A cascade of interpolation filters, complex modulators, and channel combiners allow modulation of the signal to any frequency from 47MHz to 1006MHz. Integrated direct digital frequency synthesizers allow positioning of the QAM channels with a resolution of 125Hz. The interpolation filters and resamplers provide linear phase and excellent gain flatness. Output data from the last modulator is fed to a digital-predistortion (DPD) block that can be used to correct distortion in the device’s integrated RF-DAC and output amplifiers external to the device.

II. Manufacturing Information

A. Description/Function:	High-Density Downstream Cable QAM Modulator
B. Process:	TS65, TS18
C. Number of Device Transistors:	886
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	December 10, 2013

III. Packaging Information

A. Package Type:	280-ball Flip Chip BGA
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	Conductive
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#31-4890
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	10.96°C/W
M. Multi Layer Theta Jc:	0.71°C/W

IV. Die Information

A. Dimensions:	Hybrid die
B. Passivation:	Si_3N_4/SiO_2
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 234 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.7 \times 10^{-9}$

$\lambda = 4.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS65, TS18 Process results in a FIT Rate of 0.1 @ 25°C and 1.9 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot KAEJ8AE, D/C 1251)

The CD23-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX5862AUXH+ / MAX5862BUXH+ / MAX5862CUXH+ / MAX5862DUXH+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	234	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.