RELIABILITY REPORT

FOR

MAX5908EEE

PLASTIC ENCAPSULATED DEVICES

February 27, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

Conclusion

The MAX5908 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX5908 +1V to +13.2V dual hot-swap controller provides complete protection for dual-supply systems. It allows the safe insertion and removal of circuit cards into live backplanes.

The discharged filter capacitors of the circuit card provide low impedance to the live backplane. High inrush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. The MAX5908 hot-swap controllers prevents such problems by gradually ramping up the output voltage and regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide VariableSpeed/BiLevelTM protection against short-circuit and overcurrent faults, as well as immunity against system noise and load transients. In the event of a fault condition, the load is disconnected. The MAX5908 automatically restarts after a fault.

The MAX5908 family offers a variety of options to reduce component count and design time. The device integrates an on-board charge pump to drive the gates of low-cost, external N-channel MOSFETs. The device offers integrated features like startup current regulation and current glitch protection to eliminate external timing resistors and capacitors. The MAX5908 provides an open-drain status output, an adjustable startup timer, an adjustable current limit, an uncommitted comparator, and output undervoltage/overvoltage monitoring.

Rating

The MAX5908 is available in space-saving 16-pin QSOP packages. The device is specified over the extended temperature range, -40°C to +85°C

B. Absolute Maximum Ratings

Item

•
+14V
+0.3V to (VIN_ + 6.2V)
-0.3V to the higher of (VIN1 + 0.3V) and (VIN2 + 0.3V)
$-0.3V$ to $(VIN_+ 0.3V)$
±50mA
-40°C to +85°C
-65°C to +150°C
+300°C
667mW
8.3mW/°C

II. Manufacturing Information

A. Description/Function: Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

B. Process: S8

C. Number of Device Transistors: 3230

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia, Philippines, Korea or Thailand

F. Date of Initial Production: October, 2001

III. Packaging Information

A. Package Type: 16-Lead QSOP

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1301-0029

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 80 x 77 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliablity Lab Manager) Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}} = \underbrace{\frac{1.83}{192 \text{ x } 4389 \text{ x } 80 \text{ x } 2}}_{\text{Thermal acceleration factor assuming a } 0.8\text{eV activation energy}$$

$$\lambda = 13.57 \text{ x } 10^{-9}$$
 $\lambda = 13.57 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5742) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The NP30-4 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX5908EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Str	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots. Note 2: Generic package/process data

Attachment #1

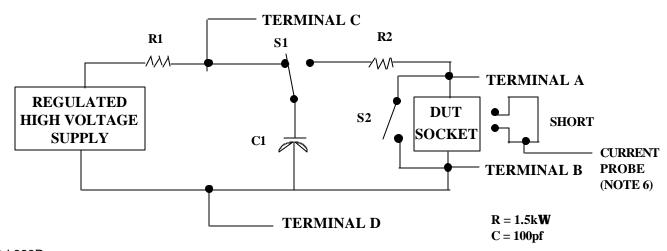
TABLE II. Pin combination to be tested. 1/2/

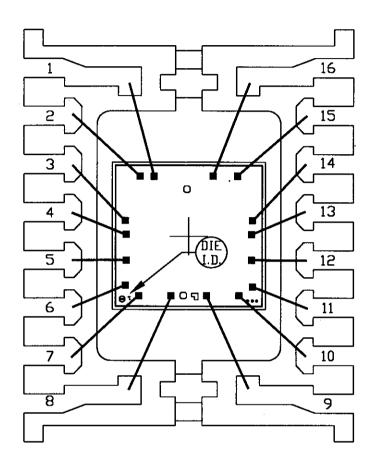
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\underline{3/}$ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E16-1		SIGNATURES	DATE CONFIDENTIAL & PROPRIETARY		
CAV./PAD SIZE:	PKG.		•	BOND DIAGRAM #:	REV:
96X130	DESIGN			05-1301-0029	Α

