RELIABILITY REPORT

FOR

MAX6120Exx

PLASTIC ENCAPSULATED DEVICES

June 17, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6120 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. ....Device Description
II. ....Manufacturing Information
III. ....Packaging Information
V. ....Quality Assurance Information
VI. ....Reliability Evaluation
IV. ....Die Information
.....Attachments

I. Device Description

A. General

The MAX6120 is the lowest-power 1.2V, precision, three-terminal voltage reference offered in a SOT23 package. Ideal for 3V battery-powered equipment where power conservation is critical, the MAX6120 is a low-power alternative to existing two-terminal shunt references. Unlike two-terminal references that throw away battery current and require an external series resistor, the MAX6120 has a 70µA maximum supply current (typically only 50µA) that is independent of the input voltage. This feature translates to maximum efficiency at all battery voltages.

The MAX6120 operates from a supply voltage as low as 2.4V, and initial accuracy is ±1% for the SOT23 package. Output voltage temperature coefficient is typically only 30ppm/°C, and is guaranteed to be less than 100ppm/°C in the SOT23 package

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VIN)	-0.3V to +12V
VOUT	-0.3V to (VIN + 0.3V)
Output Short-Circuit Duration	Continuous to Either Supply
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
3-Pin SOT23	320mW
8-Pin NSO	471mW
Derates above +70°C	
3-Pin SOT23	4.0mW/°C
8-Pin NSO	5.88mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, Micropower, Precision, 3-Terminal,1.2V Voltage Reference
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	39
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	April, 1993

III. Packaging Information

A. Package Type:	**8-Pin NSO**	**3-Pin SOT23**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate or Alloy 42
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0901-0135	# 05-0901-0136
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 44 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 240 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 9.99 \times 10^{-9}$

λ = 9.99 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. The following Burn-In Schematic (Spec. #06-5114) shows the static circuit used for this test. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RF19 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6120Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO SOT23	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

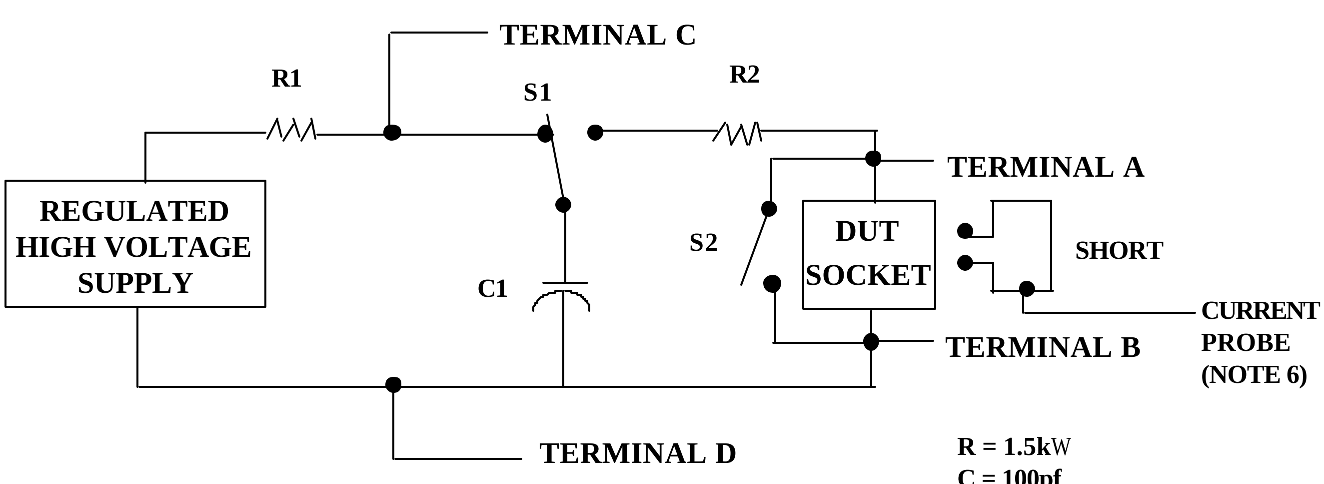
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

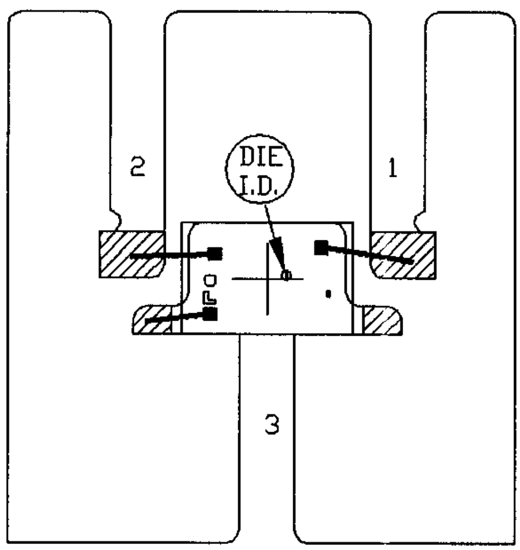
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

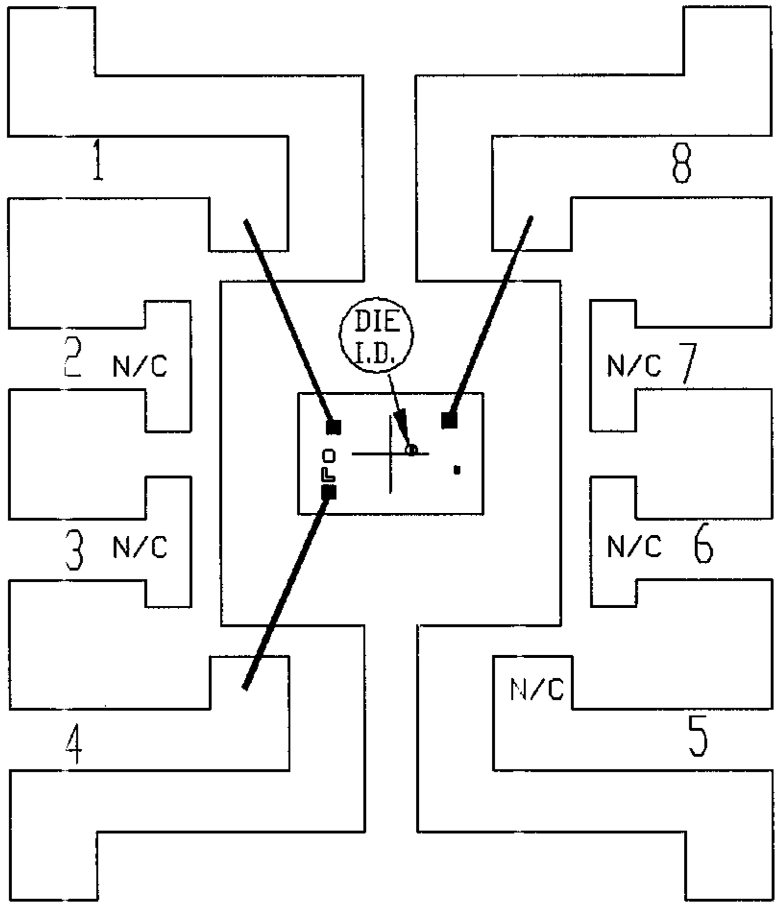
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



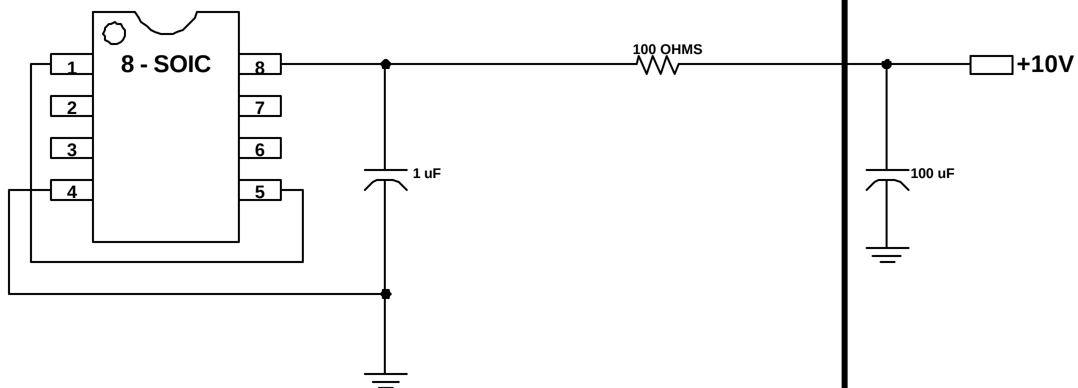


PKG.CODE: U3-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 45X32	PKG. DESIGN			BUILDSHEET NUMBER: 05-0901-0136	REV.: B



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BUILDSHEET NUMBER: 05-0901-0135	REV.: B

ONCE PER SOCKET	ONCE PER BOARD



DEVICES: MAX 6023/6012/6021/6025/6041/6045/ 6050/6120/6125/6141/6145/6150/6160/6520 **MAX. EXPECTED CURRENT = 60uA**	**DRAWN BY: HAK TAN** **NOTES:**

DOCUMENT I.D. 06-5114	**REVISION** C	***MAXIM*** **TITLE: BI Circuit (MAX6012/6021/6025/6041/6045/6050/6120/6125/6141/6145/6150/6160/6520/6023)**	**PAGE** 2 OF 3