RELIABILITY REPORT

FOR

MAX619xxA

PLASTIC ENCAPSULATED DEVICES

March 31, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager Reviewed by

Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MAX619 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Quality Assurance Information

VI.Reliability Evaluation

IV.Attachments

I. Device Description

A. General

The MAX619 step-up charge pump DC-DC converter delivers a regulated 5V \pm 4% output at 50mA over temperature. The input voltage range is 2V to 3.6V (two battery cells).

The complete MAX619 circuit fits into less than 0.1in^2 of board space because it requires only four external capacitors: two $0.22 \mu F$ flying capacitors, and $10 \mu F$ capacitors at the input and output.

Low operating supply current (150 μ A max) and low shutdown supply current (1 μ A max) make this device ideal for small, portable, and battery-powered applications. When shut down, the load is disconnected from the input.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
V _{IN} to GND	-0.3V to +5.5V
V _{OUT} to GND	-0.3V to +5.5V
SHDN to GND	$-0.3V$ to $(V_{IN} + 0.3V)$
I _{OUT} Continuous (Note 1)	120mA
Storage Temp.	-65°C to +165°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = $+70^{\circ}$)	
8-Pin PDIP	762mW
8-Pin NSO	762mW
Derates above +70°C	
8-Pin PDIP	9.4mW/°C
8-Pin NSO	9.4mW/°C

Note 1: The MAX619 is not short-circuit protected.

II. Manufacturing Information

A. Description/Function: Regulated 5V Charge-Pump DC-DC Converter

B. Process: SG1.2 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 599

D. Fabrication Location: Cailfornia or Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: February, 1994

III. Packaging Information

A. Package Type: 8-Lead NSO 8-Lead PDIP

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: # 05-2301-0002 # 05-2301-0001

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity

Per JEDEC standard J-STD-022A: Level 1 Level 1

IV. Die Information

A. Dimensions: 70 x 84 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$
(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 13.57 \text{ x } 10^{-9}$$
 $\lambda = 13.57 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5039) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY02 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1Reliability Evaluation Test Results

MAX619xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		231	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

Attachment #1

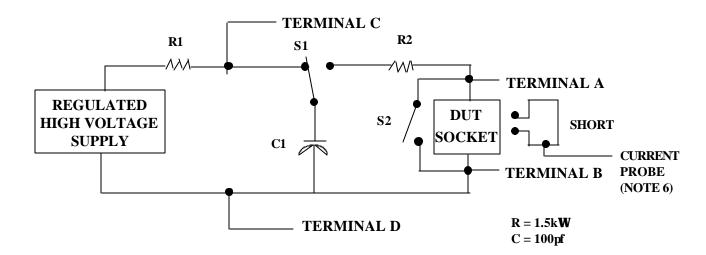
TABLE II. Pin combination to be tested. 1/2/

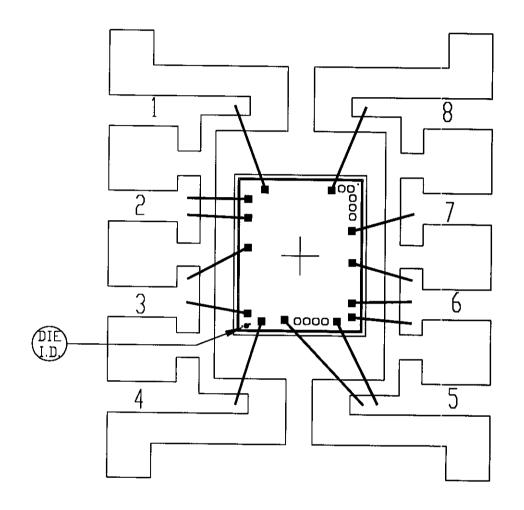
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\underline{3/}$ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S.}$ $+V_{S.}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-4		APPROVALS DATE		/VI/IXI/VI		
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BUILDSHEET NUMBER: 05-2301-0002	REV.:	

