MAX6192xESA
Rev. A

RELIABILITY REPORT

FOR

MAX6192xESA

PLASTIC ENCAPSULATED DEVICES

June 20, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6192 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6192 precision, micro-power, low-dropout voltage reference offers high initial accuracy and very low temperature coefficient through a proprietary curvature-correction circuit and laser-trimmed precision thin-film resistors.

This series-mode bandgap reference draws a maximum of only 35µA quiescent supply current, making it ideal for battery-powered instruments. It offers a supply current that is virtually immune to input voltage variations. Load-regulation specifications are guaranteed for source and sink currents up to 500µA. This device is internally compensated, making it ideal for applications that require fast settling, and is stable with capacitive loads up to 2.2nF.

B. Absolute Maximum Ratings

Item	Rating
Voltages Referenced to GND	
IN	-0.3V to +13.5V
OUT	-0.3V to (VIN + 0.3V)
Output Short Circuit to GND or IN (VIN < 6V)	Continuous
Output Short Circuit to GND or IN (VIN ≥ 6V)	60s
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SO	471mW
Derates above +70°C	
8-Pin SO	5.88mW/°C

II. Manufacturing Information

A. Description/Function: Precision, Micropower, Low-Dropout Voltage Reference

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 70

D. Fabrication Location: Oregon or California, USA

E. Assembly Location: Philippines, Thailand or Malaysia

F. Date of Initial Production: November, 1998

III. Packaging Information

A. Package Type: **8-Pin SO**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-0901-0152

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 44 x 31 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9}$$

λ = 4.52 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5387) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RF23-1 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA .

Table 1
Reliability Evaluation Test Results

MAX6192xESA

TEST ITEM	**TEST CONDITION**	**FAILURE IDENTIFICATION**	**PACKAGE**	**SAMPLE SIZE**	**NUMBER OF FAILURES**
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

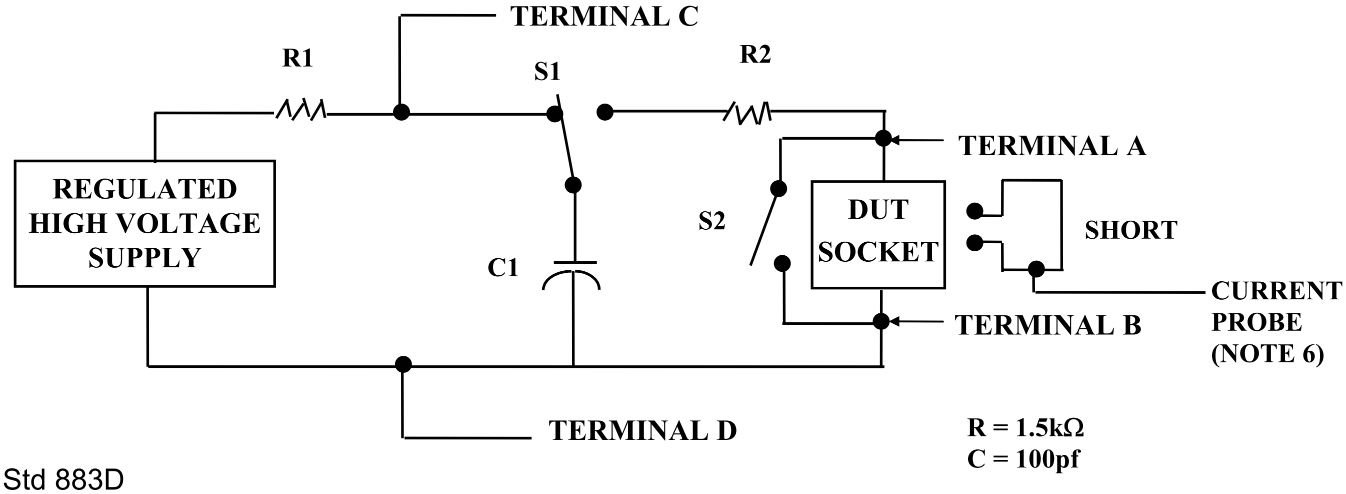
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

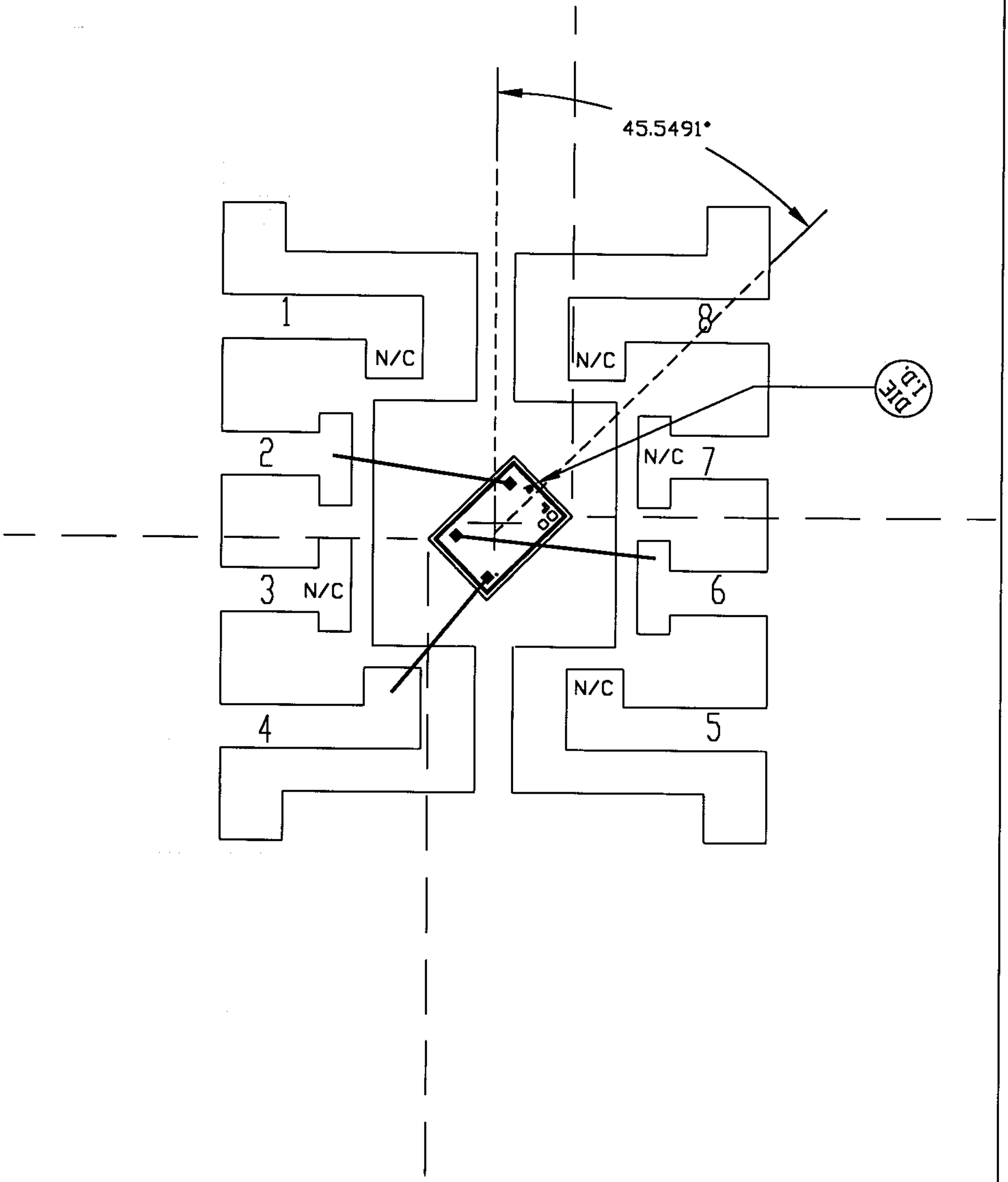
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

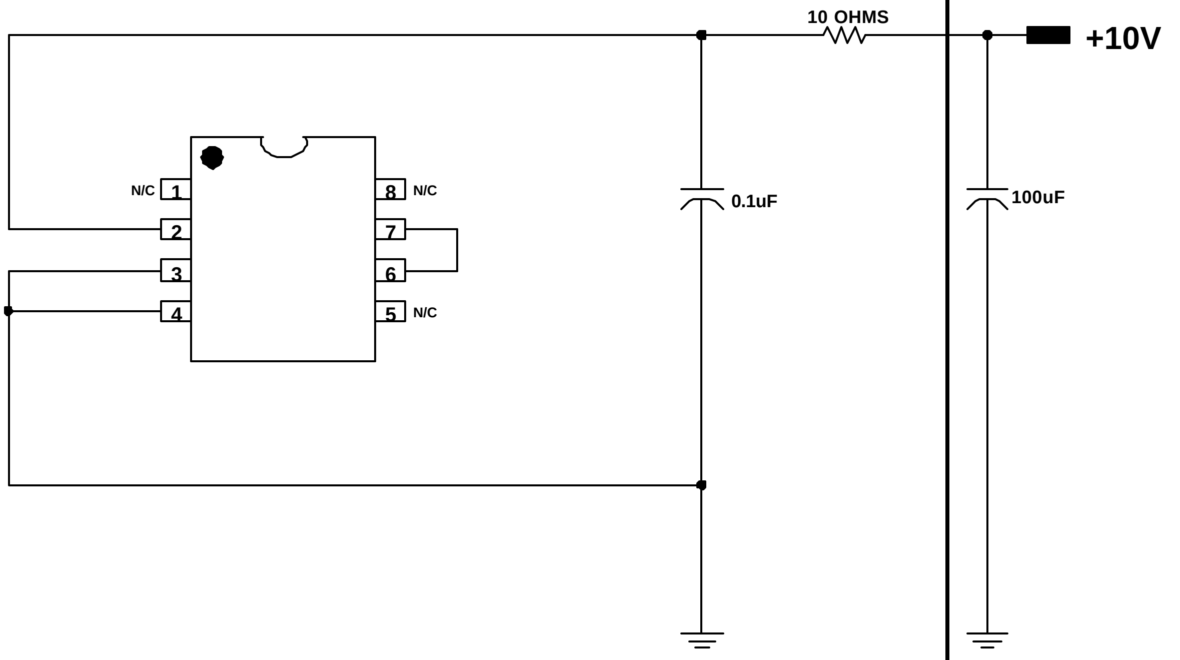
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-2		APPROVALS	DATE	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BUILDSHEET NUMBER: 05-0901-0152
				REV.: B

ONCE PER SOCKET | **ONCE PER BOARD**



DEVICES: MAX 6133/6190/6191/6192/6194/6195/6198/6126
PACKAGE: 8 - NSO
MAX. EXPECTED CURRENT = 850uA

DRAWN BY: TEK TAN

NOTES: