RELIABILITY REPORT

FOR

MAX6303ESA+T / MAX6303CPA+

PLASTIC ENCAPSULATED DEVICES

February 1, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX6303ESA+T / MAX6303CPA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6301-MAX6304 low-power microprocessor (µP) supervisory circuits provide maximum adjustability for reset and watchdog functions. The reset threshold can be adjusted to any voltage above 1.22V, using external resistors. In addition, the reset and watchdog timeout periods are adjustable using external capacitors. A watchdog select pin extends the watchdog timeout period to 500x. The reset function features immunity to power-supply transients. These four devices differ only in the structure of their reset outputs (see the *Selector Guide* in the full data sheet). The MAX6301-MAX6304 are available in the space-saving 8-pin µMAX® package, as well as 8-pin PDIP and SO packages.

II. Manufacturing Information

A. Description/Function:	+5V, Low-Power, µP Supervisory Circuits with Adjustable Reset/Watchdog
B. Process:	S3
C. Number of Device Transistors:	580
D. Fabrication Location:	USA
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	December 1, 1998

III. Packaging Information

A. Package Type:	8-pin PDIP	8-pin SOIC
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1.3 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0020	#05-1601-0021
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	110°C/W	170°C/W
K. Single Layer Theta Jc:	40°C/W	40°C/W
L. Multi Layer Theta Ja:	N/A°C/W	136°C/W
M. Multi Layer Theta Jc:	N/A°C/W	38°C/W

IV. Die Information

A. Dimensions:	68 X 58 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.04 @ 25°C and 0.69 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NNQCCQ001A, D/C 9848)

The MS07-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX6303ESA+T / MAX6303CPA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	XNQCBB001B, D/C 9637

Note 1: Life Test Data may represent plastic DIP qualification lots.