

RELIABILITY REPORT  
FOR  
**MAX6318xHUK**  
PLASTIC ENCAPSULATED DEVICES

July 26, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Quality Assurance  
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Reviewed by



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## Conclusion

The MAX6318 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX6318 microprocessor ( $\mu$ P) supervisory circuit monitors power supplies and microprocessor activity in digital systems. It offers several combinations of push/pull, open-drain, and bidirectional (such as Motorola 68HC11) reset outputs, along with watchdog and manual-reset features. This device is specifically designed to ignore fast negative transients on  $V_{CC}$ . Resets are guaranteed valid for  $V_{CC}$  down to 1V.

This device is available in 26 factory-trimmed reset threshold voltages (from 2.5V to 5V, in 100mV increments), featuring four minimum power-on reset timeout periods (from 1ms to 1.12s), and four watchdog timeout periods (from 6.3ms to 25.6s). Nine standard versions are available with an order increment requirement of 2500 pieces (see Standard Versions table); contact the factory for availability of other versions, which have an order increment requirement of 10,000 pieces.

The MAX6318 is offered in a miniature 5-pin SOT23 package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltage (with respect to GND)	
VCC	-0.3V to +6V
RESET (MAX6320/MAX6321/MAX6322 only)	-0.3V to +6V
All Other Pins	-0.3V to (VCC + 0.3V)
Input/Output Current, All Pins	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23	571mW
Derates above +70°C	
8-Pin SOT23	7.1mW/°C

## II. Manufacturing Information

A. Description:	5-Pin $\mu$ P Supervisory Circuits with Watchdog and Manual Reset
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	191
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Thailand or Malaysia
F. Date of Initial Production:	January, 1998

## III. Packaging Information

A. Package Type:	<b>5-Lead SOT23</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0034
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	61 x 87 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	$\text{SiO}_2$
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5033) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The MS13-2 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX6318xHUK**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test may represent DIP qualification packages.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

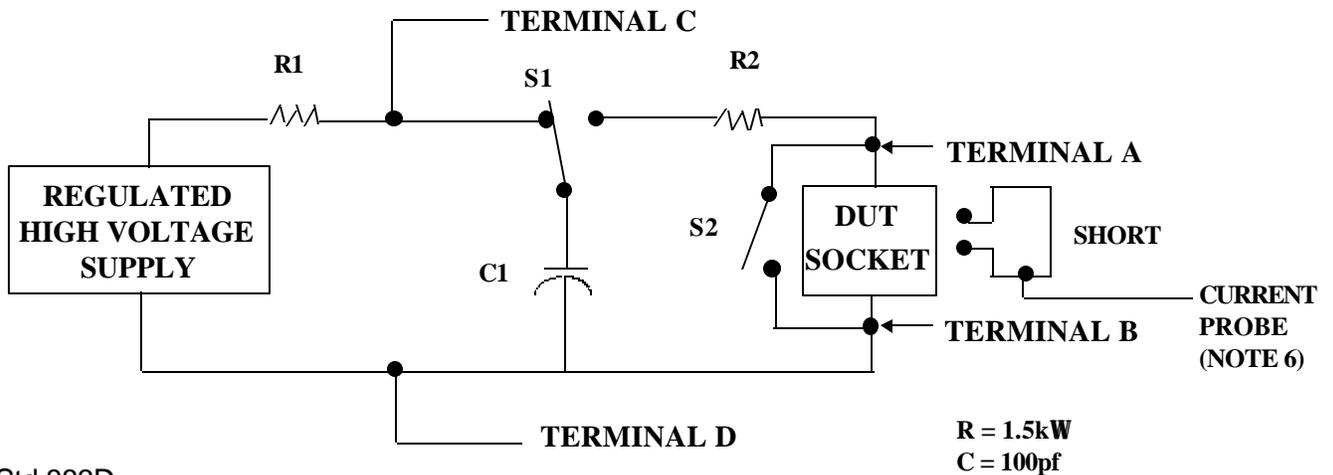
2/ No connects are not to be tested.

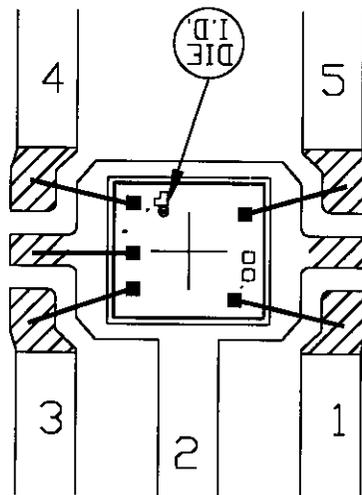
3/ Repeat pin combination 1 for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE:	U5-2	
CAV./PAD SIZE:	59x46	PKG. DESIGN

APPROVALS

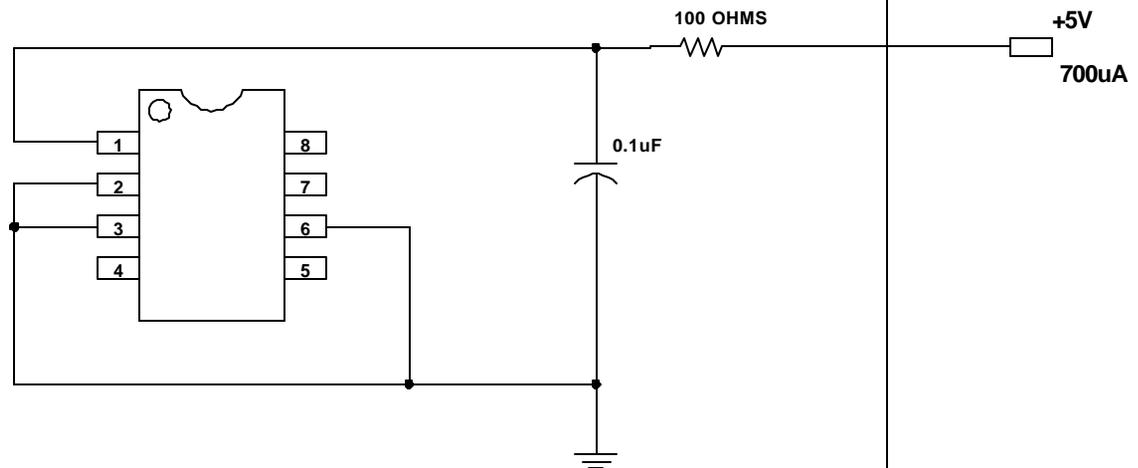
DATE

**MAXIM**

BUILDSHEET NUMBER:	REV.:
05-1601-0034	C

ONCE PER SOCKET

ONCE PER BOARD



8-DIP

DEVICES: MAX 941/809/810/823/824/825/803  
MAX 6381/6835  
MAX. EXPECTED CURRENT = 700uA AND 15uA

DRAWN BY: HAK TAN  
NOTES: 15 uA FOR MAX 6381