RELIABILITY REPORT

FOR

MAX6336US16D3+T

PLASTIC ENCAPSULATED DEVICES

October 14, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX6336US16D3+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX6335/MAX6336/MAX6337 microprocessor (µP) supervisory circuits monitor the power supplies in 1.8V to 3.3V µP and digital systems. They increase circuit reliability and reduce cost by eliminating external components and adjustments. They also feature a debounced manual-reset input. These devices perform a single function: they assert a reset signal whenever the VCC supply voltage declines below a preset threshold or whenever manual reset is asserted. Reset remains asserted for a preset timeout period after VCC has risen above the reset threshold or after manual reset is deasserted. The only difference among the three devices is their output. The MAX6336 (push/pull) and MAX6337 (open-drain) have an active-low RESET output, while the MAX6335 (push/pull) has an active-high RESET output. The MAX6335/MAX6336 are guaranteed to be in the correct state for VCC down to 0.7V. The MAX6337 is guaranteed to be in the correct state for VCC down to 1.0V. The reset comparator in these ICs is designed to ignore fast transients on VCC. Reset thresholds are factory-trimmable between 1.6V and 2.5V, in approximately 100mV increments. There are 15 standard versions available (2500 piece minimum-order quantity); contact the factory for availability of nonstandard versions (10,000 piece minimum-order quantity). For space-critical applications, the MAX6335/MAX6336/MAX6337 come packaged in a 4-pin SOT143.

II. Manufacturing Information

A. Description/Function:	4-Pin, Ultra Low-Voltage, Low-Power µP Reset Circuits with Manual Reset
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Carsem, NSEB, Unisem
F. Date of Initial Production:	January 23, 1999

III. Packaging Information

A. Package Type:	4-pin SOT
B. Lead Frame:	Alloy42
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0042
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	250*°C/W
K. Single Layer Theta Jc:	130°C/W
L. Multi Layer Theta Ja:	°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	43 X 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Jim Pedicord (Manager, Rel Operations) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.4 \times 10^{-9}$

λ = 13.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S12 Process results in a FIT Rate of 12.5 @ 25C and 192.25 @ 55C, data limited (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The MS16-1 die type has been found to have all pins able to withstand a HBM transient pulse of 2500V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of 250ma.

Table 1
Reliability Evaluation Test Results

MAX6336US16D3+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data