RELIABILITY REPORT

FOR

MAX6353SYUK

PLASTIC ENCAPSULATED DEVICES

March 5, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6353SY successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6353 microprocessor (µP) supervisor with multiple reset voltages significantly improves system reliability and accuracy compared to separate ICs or discrete components. If any input supply voltage drops below its associated preset threshold, all reset outputs are asserted. In addition, the outputs are valid as long as either input supply voltage remains greater than +1.0V.

This device has an active-low debounced manual reset input. The MAX6353 offers an active-low, push-pull reset output referenced to $V_{CC}1$

The device is available in 5-pin SOT23 package and operates over the extended (-40°C to +85°C) temperature range.

B. Absolute Maximum Ratings

Item	Rating
VCC1, VCC2 to GND	-0.3V to +6V
RST , MR , WDI, RST1 , RSTIN	-0.3V to (VCC5 + 0.3V)
Input/Output Current, All Pins	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
5-pin SOT23	571mW
Derates above +70°C	
5-pin SOT23	7.1mW/°C

II. Manufacturing Information

A. Description/Function:	Dual-Voltage µP Supervisory Circuits
B. Process:	S12 – Silicon Gate 1.2 micron CMOS
C. Number of Device Transistors:	855
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	October, 1999

III. Packaging Information

A. Package Type:	**5-Lead SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Bonding Diagram	05-1601-0069
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	35 x 55 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 150 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 7.24 \times 10^{-9}$ $\lambda = 7.24$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of ts processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5449) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS19-8 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX6353SYUK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		150	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

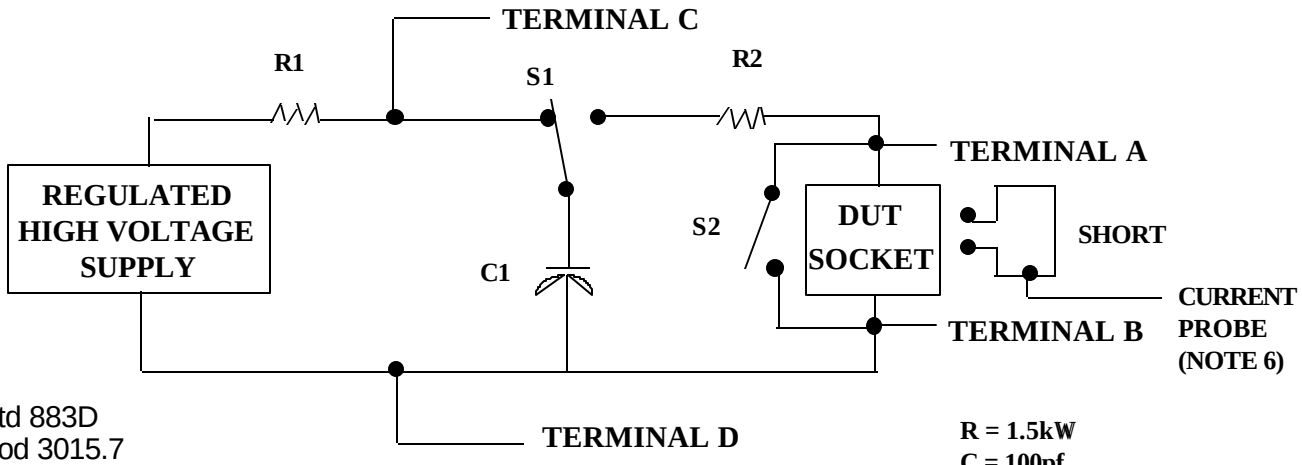
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

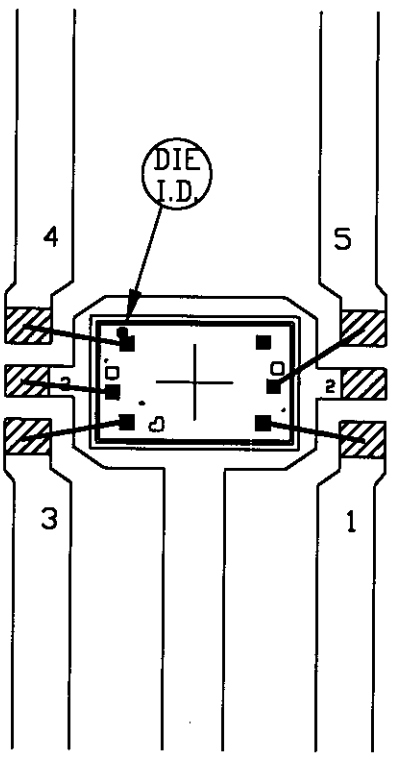
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



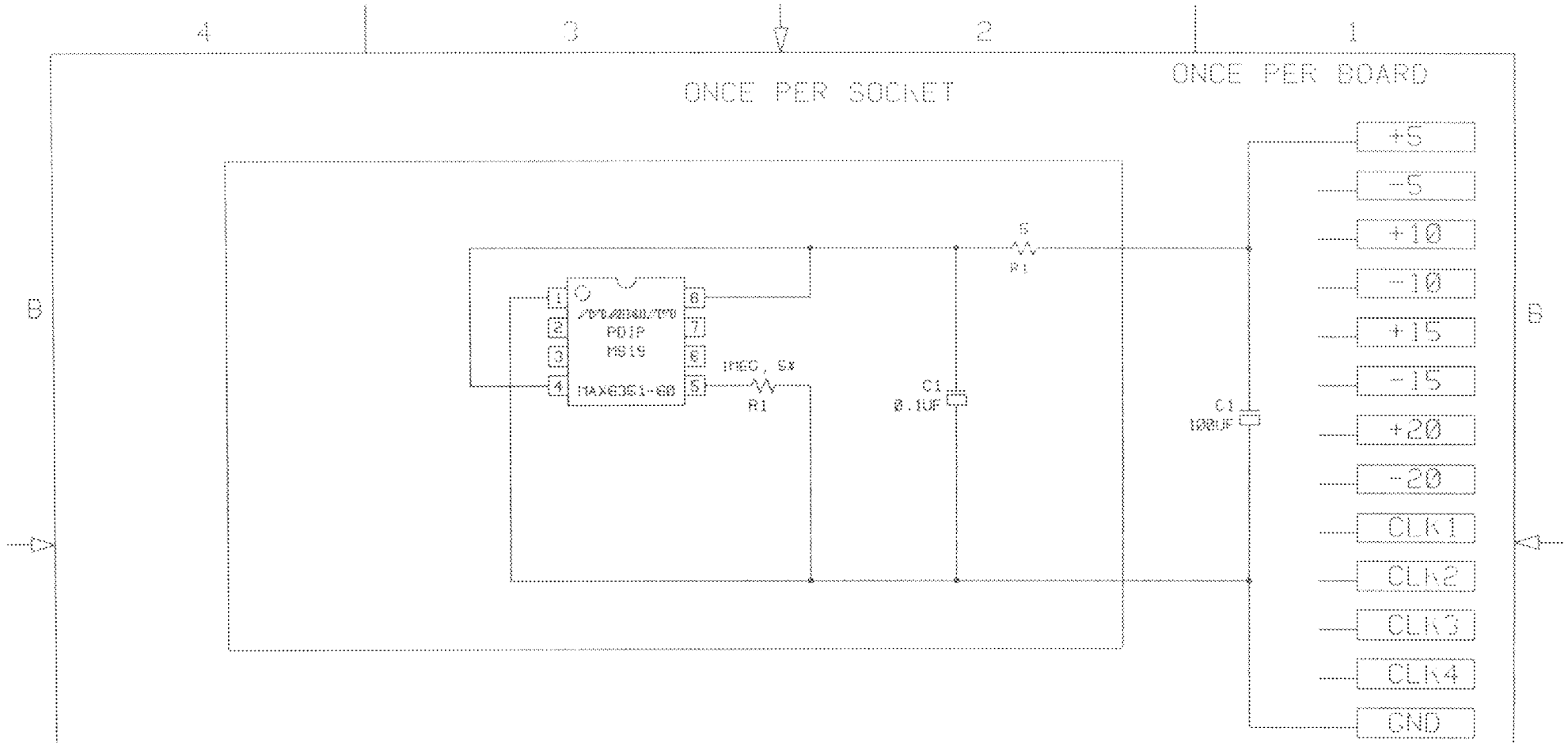
Mil Std 883D
Method 3015.7
Notice 8



▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64X45	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0069 / REV.: A



NOTE:

1. TEMPERATURE : 155 C
2. TIME 168 HOURS MIN OR EQUIVALENT
3. PACKAGE: 8-PIN PDIP
4. MAX CURRENT PER DEVICE = 200UA
5. ALL COMPONENTS & MATERIALS MUST WITHSTAND 150C CONTINUOUS
7
8
9

SPEC NO. 06-5449

DATE 2/8/99

APPROVED BY: T.B. DATE 5/20/99

MAXIM BURN-IN SCHEMATIC

PRODUCT MAX6351-6360
MAX6326/27/28
MAX6346/47/48