RELIABILITY REPORT

FOR

MAX6392KAxx

PLASTIC ENCAPSULATED DEVICES

May 18, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6392 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

The MAX6392 microprocessor (µP) supervisory circuit provides sequenced logic reset outputs for multicomponent or dual-voltage systems. The device can monitor two supply voltages and time-sequence two reset outputs to control the order in which system components are turned on and off. The MAX6392 increases system reliability and reduces circuit complexity and cost compared to separate ICs or discrete components.

The MAX6392 monitors V_{CC} as the master reset supply. Both RESET1-bar and RESET2-bar are asserted whenever V_{CC} drops below the selected factory-fixed reset threshold voltage. RESET1 remains asserted as long as V_{CC} is below the threshold and deasserts 140ms (min) after V_{CC} exceeds the thresholds.

RESET IN2 is monitored as the secondary reset supply and is adjustable with an external resistive-divider network. RESET2-bar is asserted whenever either V_{CC} or RESET IN2 is below the selected thresholds. RESET2-bar remains asserted 140ms (min) or a capacitor-adjustable time period after V_{CC} and RESET IN2 exceed their thresholds. RESET2 is always deasserted after RESET1-bar during system power-up and is always asserted before RESET1-bar during power-down.

The MAX6392 includes an active-low manual reset input (MR) that asserts both RESET1-bar (push-pull) and RESET2 (open drain).

The MAX6392 is available in small 8-pin SOT23 package and is specified over the -40°C to +85°C extended temperature range.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6.0V
RESET1 (MAX6392), RESET IN2, CSRT, MR to GND	-0.3V to (VCC + 0.3V)
Input Current (VCC, GND, CSRT, R1, R2, MR)	±20mA
Output Current (RESET1, RESET2)	±20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SOT23	421mW
Derates above +70°C	
8-Pin SOT23	5.26mW/°C

II. Manufacturing Information

A. Description/Function:	Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs
B. Process:	B8
C. Number of Device Transistors:	810
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia and USA
F. Date of Initial Production:	October, 2001

III. Packaging Information

A. Package Type:	**8-Lead SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0137
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	64 x 24 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Reliablity Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

└ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ λ= 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5689) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS59-1 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX6392KAxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

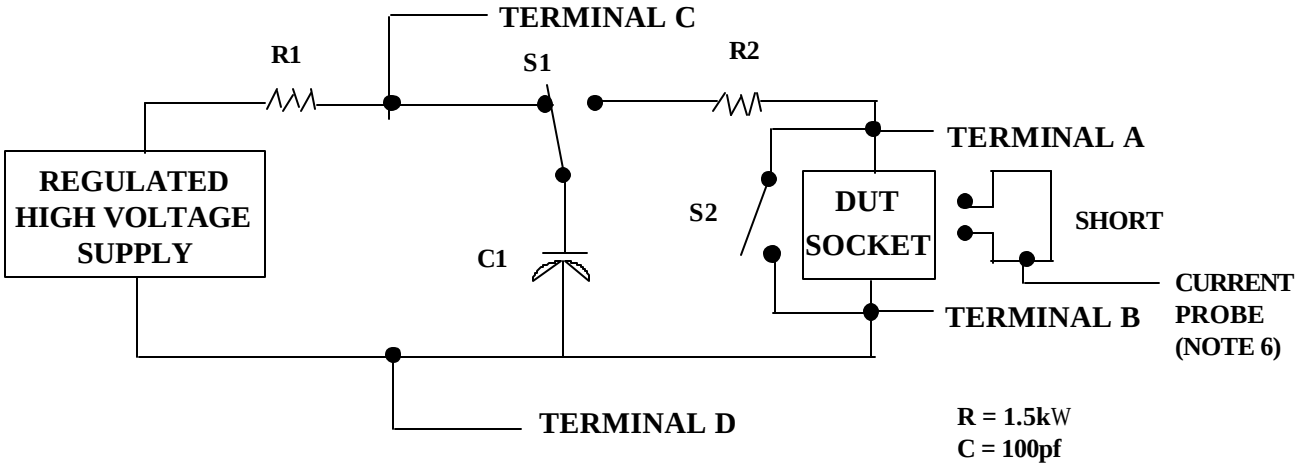
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

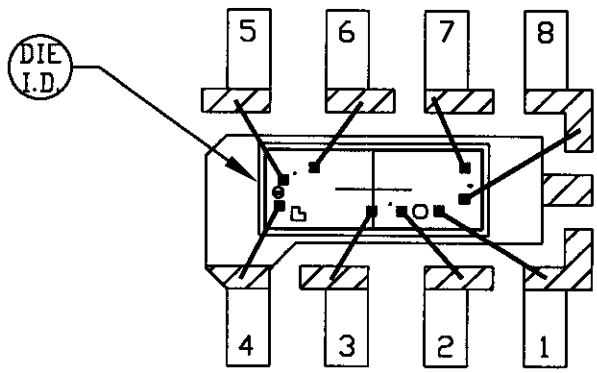
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





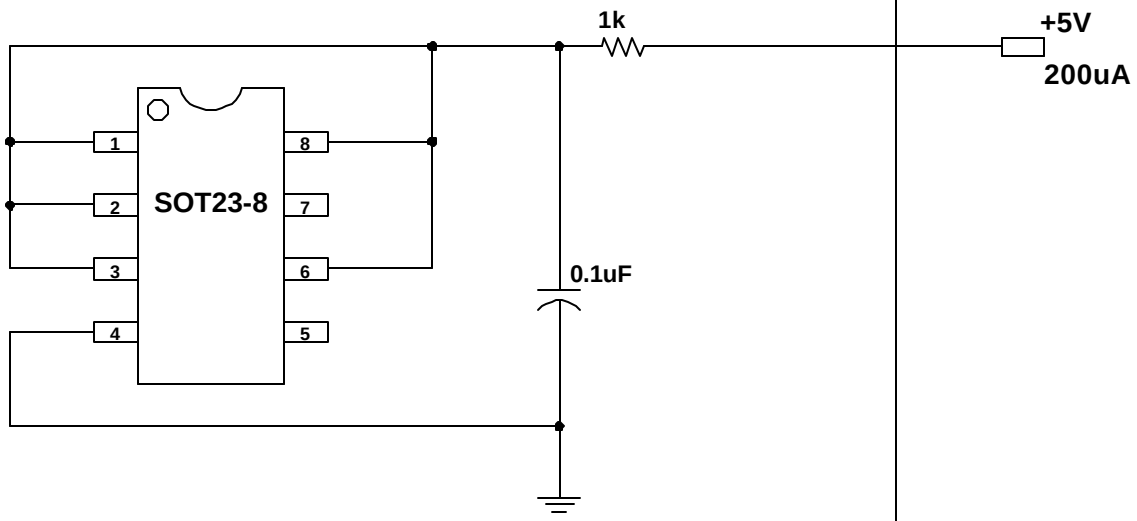
NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: K8-5		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 88x28	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0137 / REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6391/ 6392

MAX. EXPECTED CURRENT = 200uA

DRAWN BY: HAK TAN

NOTES: