

RELIABILITY REPORT
FOR
MAX6646MUA
PLASTIC ENCAPSULATED DEVICES

January 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6646 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6646 is a precise, two-channel digital temperature sensor. The device accurately measures the temperature of its own die and a remote PN junction, and reports the temperature in digital form using a 2-wire serial interface. The remote PN junction is typically the emitter-base junction of a common-collector PNP on a CPU, FPGA, or ASIC.

The 2-wire serial interface accepts standard system management bus (SMBus™) write byte, read byte, send byte, and receive byte commands to read the temperature data and to program the alarm thresholds. To enhance system reliability, the MAX6646 includes an SMBus timeout. A fault queue prevents the ALERT-bar and OVERT-bar outputs from setting until a fault has been detected one, two, or three consecutive times (programmable).

The MAX6646 provides two system alarms: ALERT-bar and OVERT-bar. ALERT-bar asserts when any of four temperature conditions are violated: local overtemperature, remote overtemperature, local undertemperature, or remote undertemperature. OVERT-bar asserts when the temperature rises above the value in either of the two OVERT-bar limit registers. The OVERT-bar output can be used to activate a cooling fan, or to trigger a system shutdown.

Measurements can be done autonomously, at the programmed conversion rate, or in a single-shot mode. The adjustable conversion rate allows optimizing supply current and temperature update rate to match system needs.

Remote accuracy is $\pm 1^\circ\text{C}$ maximum error between $+60^\circ\text{C}$ and $+145^\circ\text{C}$ with no calibration needed. The MAX6646 operates from -55°C to $+125^\circ\text{C}$, and measures temperatures between 0°C and $+145^\circ\text{C}$. The MAX6646 is available in an 8-pin μMAX package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
All Voltages Referenced to GND	
VCC	-0.3V to +6V
DXP	-0.3V to (VCC + 0.3V)
DXN	-0.3V to +0.8V
SCLK, SDA, ALERT, OVERT	-0.3V to +6V
SDA, ALERT, OVERT Current	-1mA to +50mA
DXN Current	$\pm 1\text{mA}$
Junction Temperature	$+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Continuous Power Dissipation (TA = $+70^\circ\text{C}$)	
8-Pin μMAX	471mW
Derates above $+70^\circ\text{C}$	
8-Pin μMAX	5.9mW/ $^\circ\text{C}$

II. Manufacturing Information

- A. Description/Function: +145°C Precision SMBus-Compatible Remote/ Local Sensors with Overtemperature Alarms
- B. Process: B8 (Standard 0.8 micron silicon gate CMOS)
- C. Number of Device Transistors: 14,764
- D. Fabrication Location: California, USA
- E. Assembly Location: Malaysia
- F. Date of Initial Production: July, 2003

III. Packaging Information

- A. Package Type: **8-Pin μ MAX**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Non-Conductive Epoxy
- E. Bondwire: Gold (1 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-2901-0050
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

- A. Dimensions: 75 x 88 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 0.8 microns (as drawn)
- F. Minimum Metal Spacing: 0.8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9}$$

$$\lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5975) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The TS47-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX6646MUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

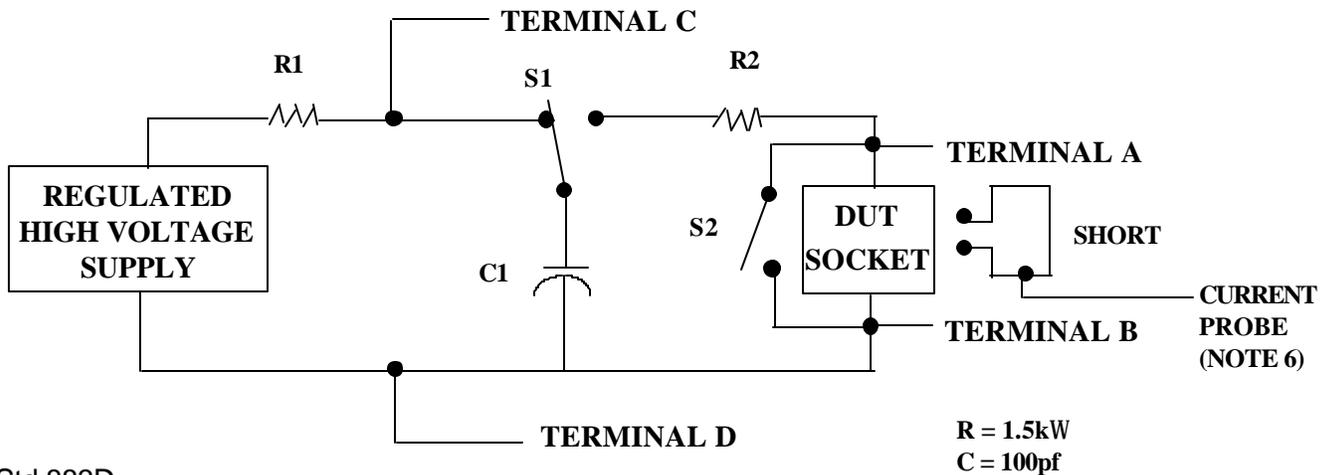
2/ No connects are not to be tested.

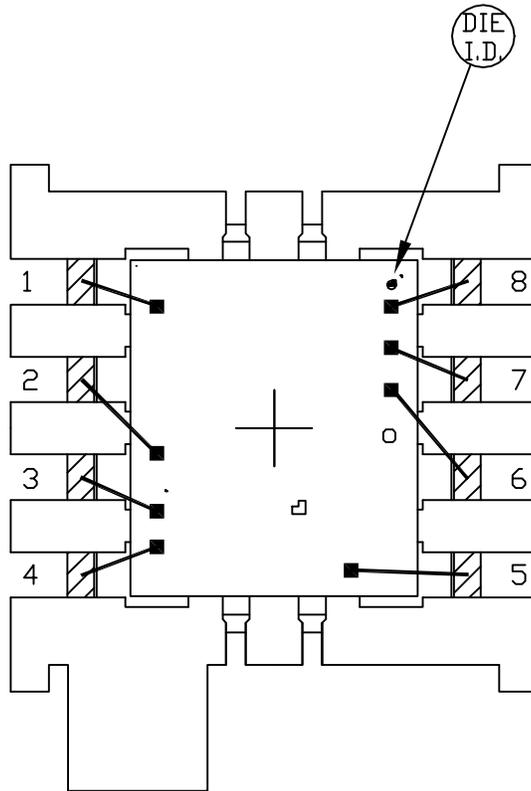
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





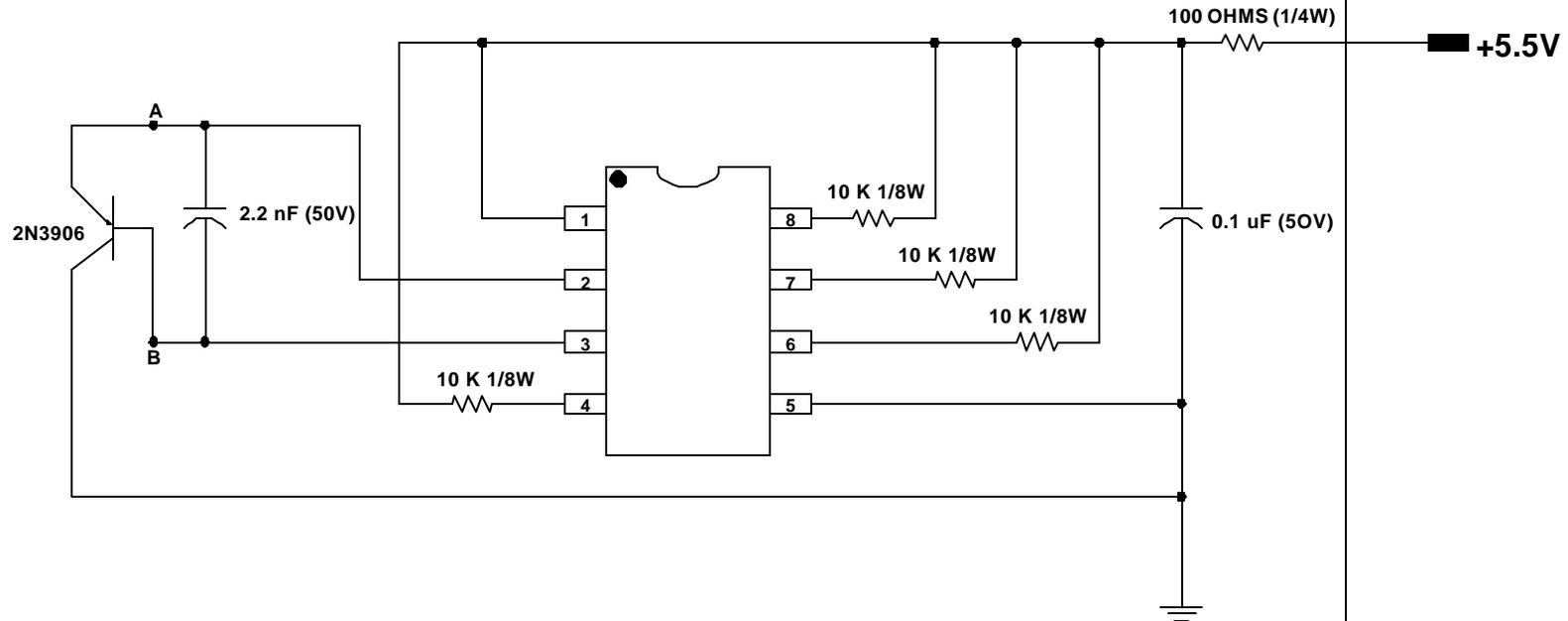
USE NON-CONDUCTIVE EPOXY

 BONDING AREA

PKG. CODE: U8C-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: CHIP ON LEAD	PKG. DESIGN			BOND DIAGRAM #: 05-2901-0050	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX6692
PACKAGE: 8-uMAX
MAX. EXPECTED CURRENT = 5mA

DRAWN BY: TEK TAN
NOTES: All resistors are once per column.