RELIABILITY REPORT

FOR

MAX6703xKA

PLASTIC ENCAPSULATED DEVICES

October 24, 2005

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6703 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX6703 microprocessor (µP) supervisory circuit reduces the complexity and components required to monitor power-supply functions in µP systems. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The MAX6703 provides four functions: a reset output during power-up, power-down and brownout conditions; an independent watchdog output that goes low if the watchdog input has not been toggled within 1.6s; a 0.62V threshold detector for power-fail warning; and an active-low manual reset input.

The MAX6703 monitors three supply voltages (one fixed threshold and two adjustable) to drive a single reset output and include a manual reset input and a watchdog timer with an independent output.

B. Absolute Maximum Ratings

Item	Rating
VCC	-0.3V to +6V
Open-Drain /RESET, /WDO, /PFO	-0.3V to +6V
/MR,WDI,PFI,RST_IN1,RST_in2	-0.3V to (VCC + 0.3V)
Input Current (VCC)	20mA
Output Current (/RESET, RESET, /PFO, /WDO)	20mA
Operating Temp Range	-40^0C to $+125^0$C
Storage Temp Range	-65^0C to $+150^0$C
Lead Temp Range (soldering, 10s)	$+300^0$C
Power Dissipation	
8-Pin SOT23	714mW
Derates above +70°C	
8-Pin SOT23	8.9mW/°C

II. Manufacturing Information

A. Description/Function:	Low Voltage Supervisor with Power Fail In/Out, Manual Reset & Watchdog Timer
B. Process:	S8/B8
C. Number of Device Transistors:	716
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**8-Lead SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0136
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	62 x 24 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliablity Lab Manager)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5687) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**). Current monitor data for the S8/B8 Process results in a FIT Rate of 0.27 @ 25C and 4.64 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS51-6 die type has been found to have all pins able to withstand a transient pulse of +/-2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

Table 1
Reliability Evaluation Test Results

MAX6703xKA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

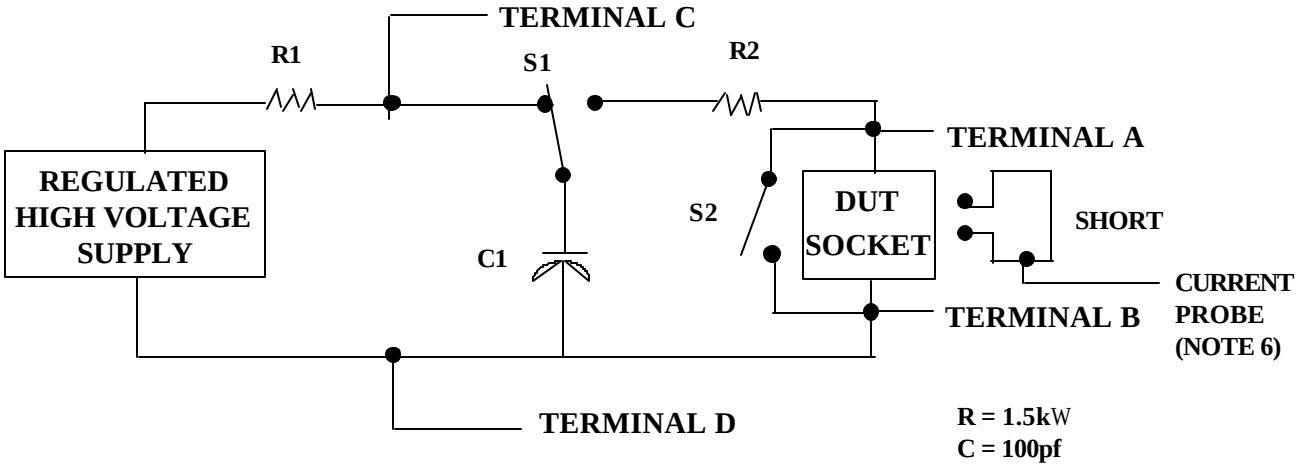
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

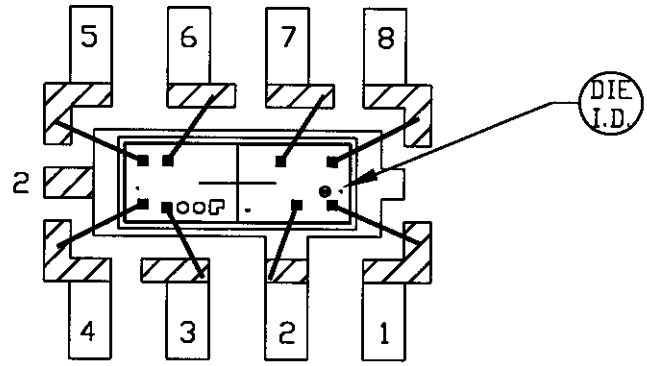
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





USE NON-CONDUCTIVE EPOXY

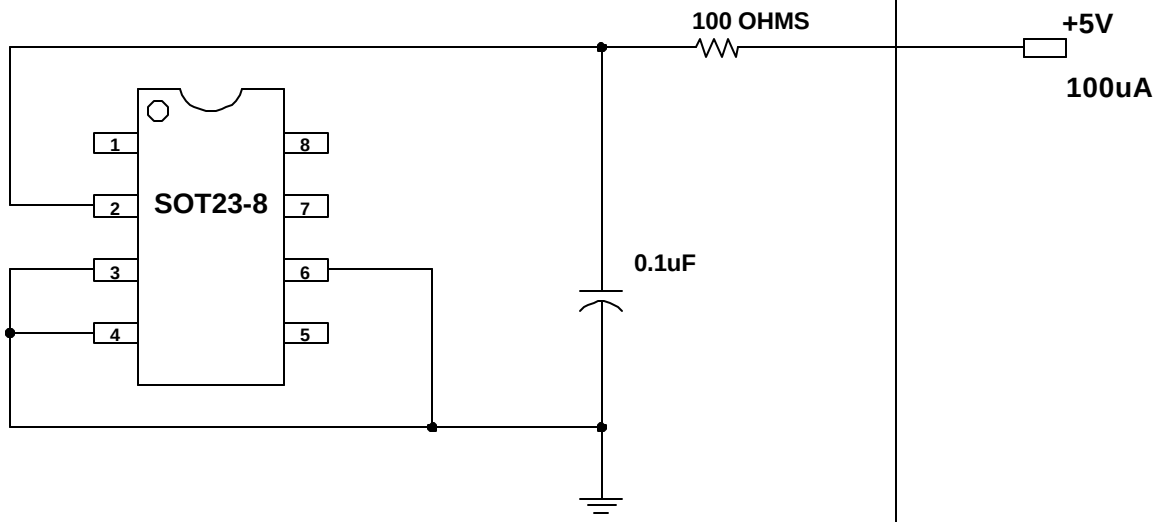
NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: K8-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 75x28	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0136 / REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6705

MAX. EXPECTED CURRENT = 100uA