RELIABILITY REPORT

FOR

MAX6808xxxx

PLASTIC ENCAPSULATED DEVICES

March 8, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6808 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6808 precision voltage detector is ideal for accurate monitoring of power supplies in digital systems. It provides circuit reliability and reduce total cost by eliminating external components and adjustments.

The MAX6808 asserts a reset signal whenever the supply voltage (V_{CC}) falls below the factory-preset, ±2% accurate threshold. Internal hysteresis ensures stable switching. The MAX6808 is available in 4.6V and 2.6V thresholds and the features an active-low, open-drain RESET-bar output. RESET-bar is valid for V_{CC} down to 1V.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6V
/RESET to GND	-0.3V to (VCC + 0.3V)
MR to GND (SOT143 package only)	-0.3V to 6.0V
Input Current, VCC	+/-20mA
Output Current, /RESET	+/-20mA
Rate of Rise, VCC	100V/uS
Storage Temp.	-65°C to +150°C
Lead Temp (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
3-Pin SOT23	320mW
3-Pin SC70	174mW
4-Pin SOT143	320mW
8-Pin uMAX	362mW
8-Pin NSO	471mW
Derates above +70°C	
3-Pin SOT23	4.0mW/°C
3-Pin SC70	2.17mW/°C
4-Pin SC143	4.0mW/°C
8-Pin uMAX	4.5mW/°C
8-Pin NSO	5.9mW/°C

II. Manufacturing Information

A. Description/Function:	Voltage Detectors
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	72
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Korea, Philippines, Thailand or Malaysia
F. Date of Initial Production:	January, 1999

III. Packaging Information

A. Package Type:	**3-Lead SOT23**	**3-Lead SC70**	**4-Lead SOT143**
B. Lead Frame:	Alloy 42	Alloy 42	Alloy 42
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0062	#05-1601-0064	#05-1601-0064
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level

A. Package Type:	**8-Lead uMAX**	**8-Lead SO**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0149	#05-1601-0148
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 80 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 14.10 \times 10^{-9}$

$\lambda = 14.10$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS22 die type has been found to have all pins able to withstand a transient pulse of ± 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX6808xxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SC70 SOT23 SOT143 uMAX	77 398 180 235	0 0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

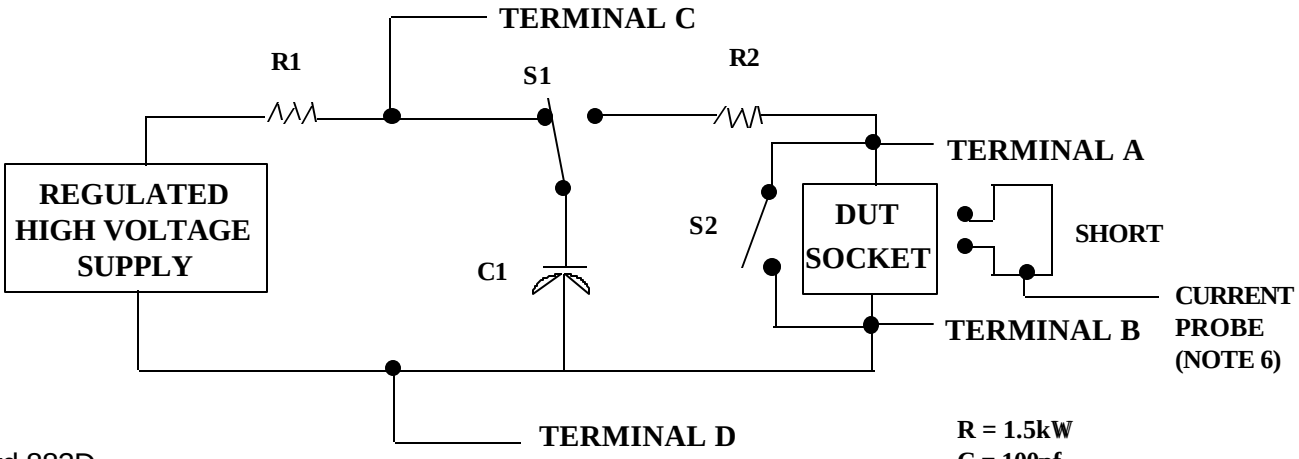
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

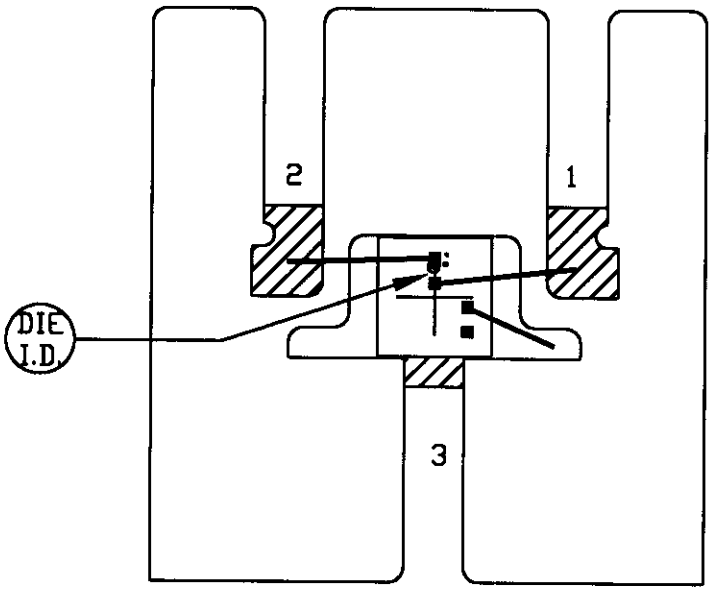
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

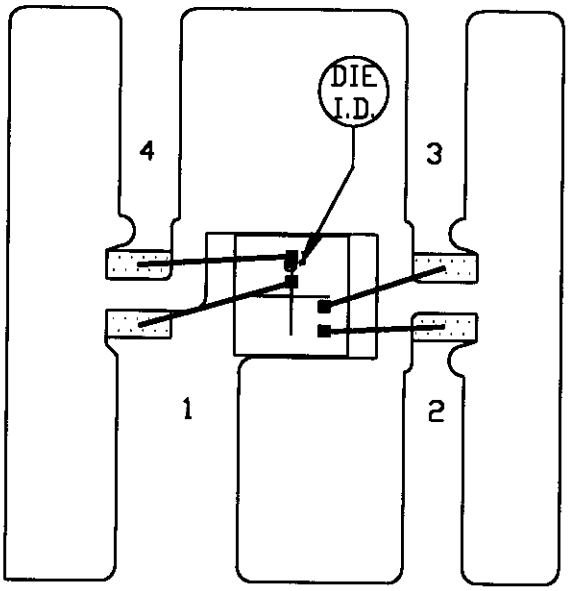
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



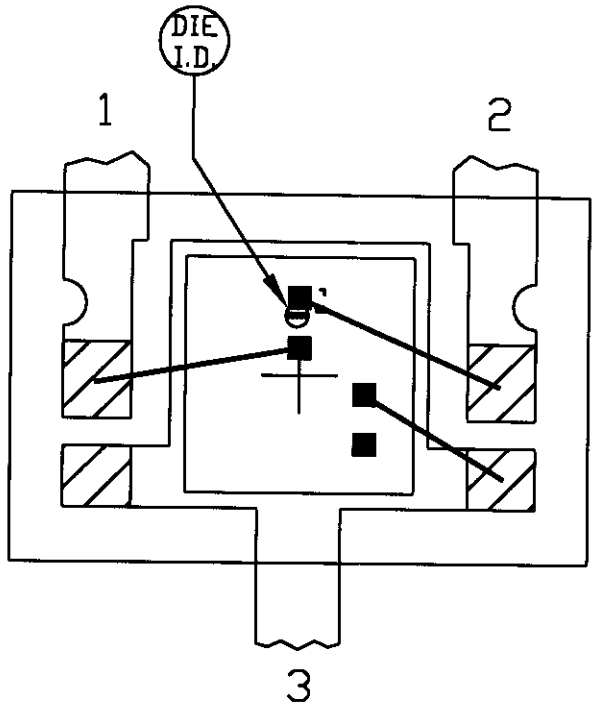
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: U3-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 45X32	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0062	REV.: A



PKG.CODE: U4-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 45X32	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0063 / REV.: A

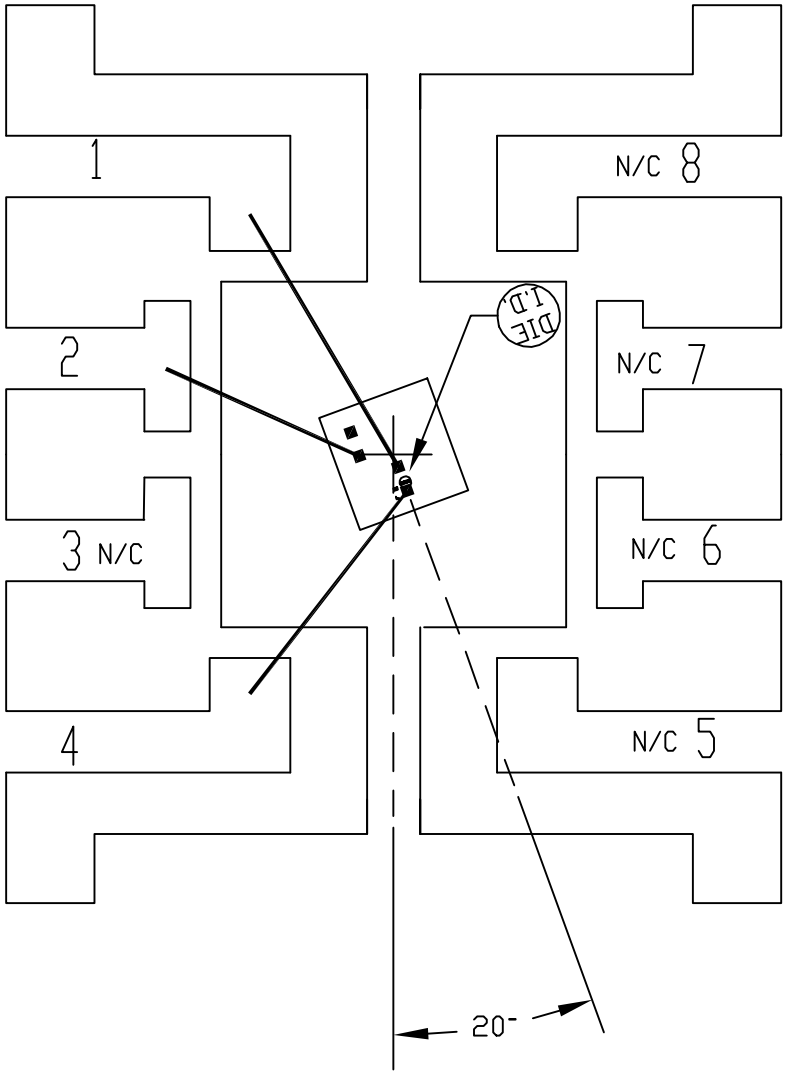


SCALE: 40x

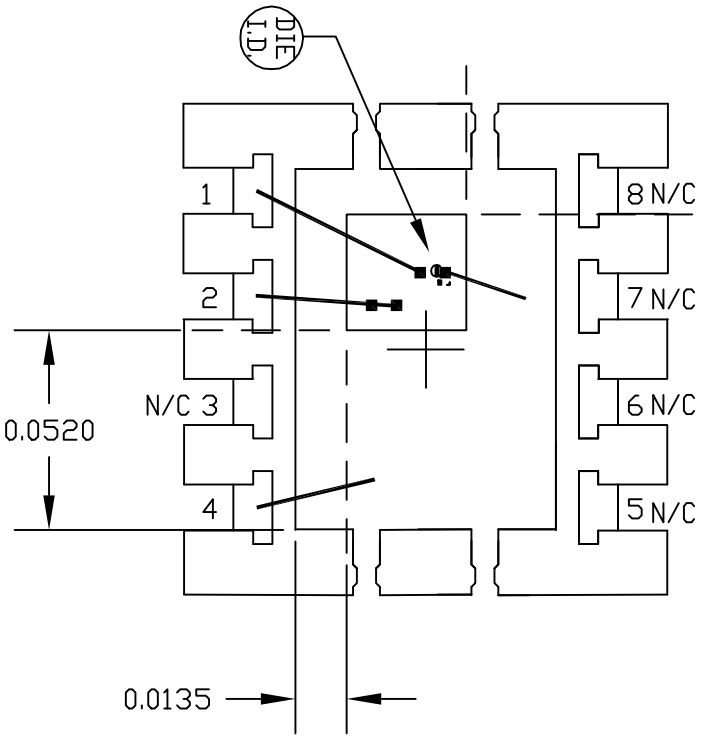
CAVITY DOWN

BONDABLE AREA

PKG.CODE: X3-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 34x35	PKG.		4/27/99	BUILDSHEET NUMBER: 05-1601-0064 REV.: B
	DESIGN		4/28/99	



PKG. CODE: S8-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 90 X 90	PKG.			BOND DIAGRAM #: 05-1601-0148	REV: A
	DESIGN				



PKG. CODE: U8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68×94	PKG.			BOND DIAGRAM #: 05-1601-0149	REV: A
	DESIGN				