

RELIABILITY REPORT
FOR
MAX6952EAX+
PLASTIC ENCAPSULATED DEVICES

October 8, 2014

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX6952EAX+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6952 is a compact cathode-row display driver that interfaces microprocessors to 5 x 7 dot-matrix LED displays through an SPI-compatible serial interface. The MAX6952 drives up to four digits (140 LEDs). Included on chip are an ASCII 104-character font, multiplex scan circuitry, column and row drivers, and static RAM that stores each digit, as well as font data for 24 user-definable characters. The segment current for the LEDs is set by an internal digit-by-digit digital brightness control. The device includes a low-power shutdown mode, segment blinking (synchronized across multiple drivers, if desired), and a test mode that forces all LEDs on. The LED drivers are slew rate limited to reduce EMI. For a 2-wire interfaced version, refer to the MAX6953 data sheet. An EV kit is available for the MAX6952.

II. Manufacturing Information

A. Description/Function:	4-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 x 7 Matrix LED Display Driver
B. Process:	TS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines, Malaysia
F. Date of Initial Production:	April 27, 2002

III. Packaging Information

A. Package Type:	36-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3301-0015
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	84.7457627119°C/W
K. Single Layer Theta Jc:	19.3°C/W
L. Multi Layer Theta Ja:	57.6°C/W
M. Multi Layer Theta Jc:	19.3°C/W

IV. Die Information

A. Dimensions:	126X183 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50um
F. Minimum Metal Spacing:	0.50um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 24.4 \times 10^{-9}$$

$$\lambda = 24.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.3 @ 25C and 5.07 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot K5W0BQ002D, D/C 0142)

The DW41 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA.

Table 1
Reliability Evaluation Test Results

MAX6952EAX+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0	K5W0BQ002D, D/C 0142

Note 1: Life Test Data may represent plastic DIP qualification lots