RELIABILITY REPORT

FOR

**MAX6954Axx**

PLASTIC ENCAPSULATED DEVICES

June 21, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

## Conclusion

The MAX6954 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents



## I. Device Description

### A. General

The MAX6954 is a compact display driver that interfaces microprocessors to a mix of 7-segment, 14-segment, and 16-segment LED displays through an SPI™- or QSPI™-compatible 4-wire serial interface. The serial interface may be cascaded through multiple devices. The MAX6954 drives up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, or 128 discrete LEDs, while functioning from a supply voltage as low as 2.7V. The driver includes five I/O expander (or GPIO) lines, some or all or which may be configured as a key-switch reader, which automatically scans and debounces a matrix of up to 32 switches.

Included on chip are full 14- and 16-segment ASCII 104-character fonts, a hexadecimal font for 7-segment displays, multiplex scan circuitry, anode and cathode drivers, and static RAM that stores each digit. The maximum segment current for the display digits is set using a single external resistor. Digit intensity can be independently adjusted using the 16-step internal digital brightness control. The MAX6954 includes a low-power shutdown mode, a scan-limit register that allows the user to display from 1 to 16 digits, segment blinking (synchronized across multiple drivers, if desired), and a test mode, which forces all LEDs on. The LED drivers are slew-rate limited to reduce EMI.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Voltage (with Respect to GND) | |
| V+ | -0.3V to +6V |
| All Other Pins | -0.3V to (V+ + 0.3V) |
| Current | |
| O0–O7 Sink Current | 935mA |
| O0–O18 Source Current | 55mA |
| DIN, CLK, CS, OSC, DOUT, BLINK, OSC_OUT, ISET | 20mA |
| P0, P1, P2, P3, P4 | 40mA |
| GND | 1A |
| Operating Temperature Range (TMIN to TMAX) | -40°C to +125°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 36-Pin SSOP | 941mW |
| 40-Pin PDIP | 1333mW |
| Derates above +70°C | |
| 36-Pin SSOP | 11.8mW/°C |
| 40-Pin PDIP | 16.7mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 4-Wire Interfaced, 2.7V to 5.5V LED Display Driver with I/O Expander and Key Scan |
| B. Process: | TC05 (0.5 micron CMOS) |
| C. Number of Device Transistors: | 57,480 |
| D. Fabrication Location: | Taiwan, USA |
| E. Assembly Location: | Philippines or Korea |
| F. Date of Initial Production: | February, 2003 |

## III. Packaging Information

| | | |
|---|---|---|
| A. Package Type: | **36-Lead SSOP** | **40-Lead PDIP** |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-Filled Epoxy | Silver-Filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-3301-0026 | # 05-3301-0027 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 131 x 147 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/Si/Cu (Aluminum/ Silicon/ Copper) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal 1: 0.6 microns; Metal 2: 0.7 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal 1: 0.6 microns; Metal 2: 0.7 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts:

| | |
|---|---|
| Jim Pedicord | (Manager, Rel Operations) |
| Bryan Preeshl | (Executive Director of QA) |
| Kenneth Huening | (Vice President) |

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 41 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 26.49 \times 10^{-9}$ $\lambda = 26.49$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5946.) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DW42 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

**Table 1**
Reliability Evaluation Test Results

**MAX6954Axx**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 41 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | PDIP<br>SSOP | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

**Attachment #1**

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

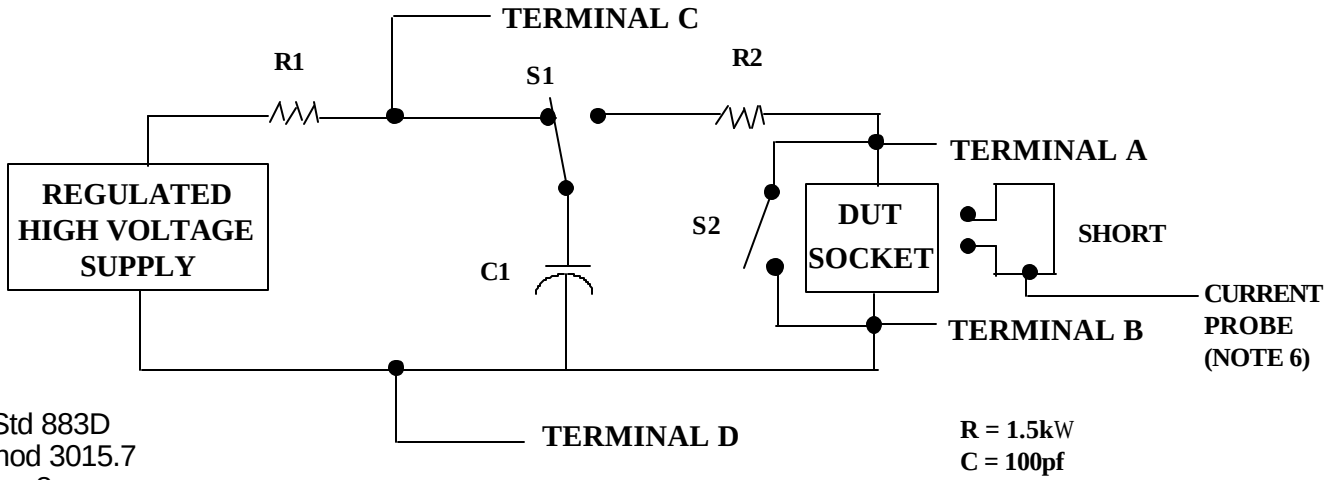
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

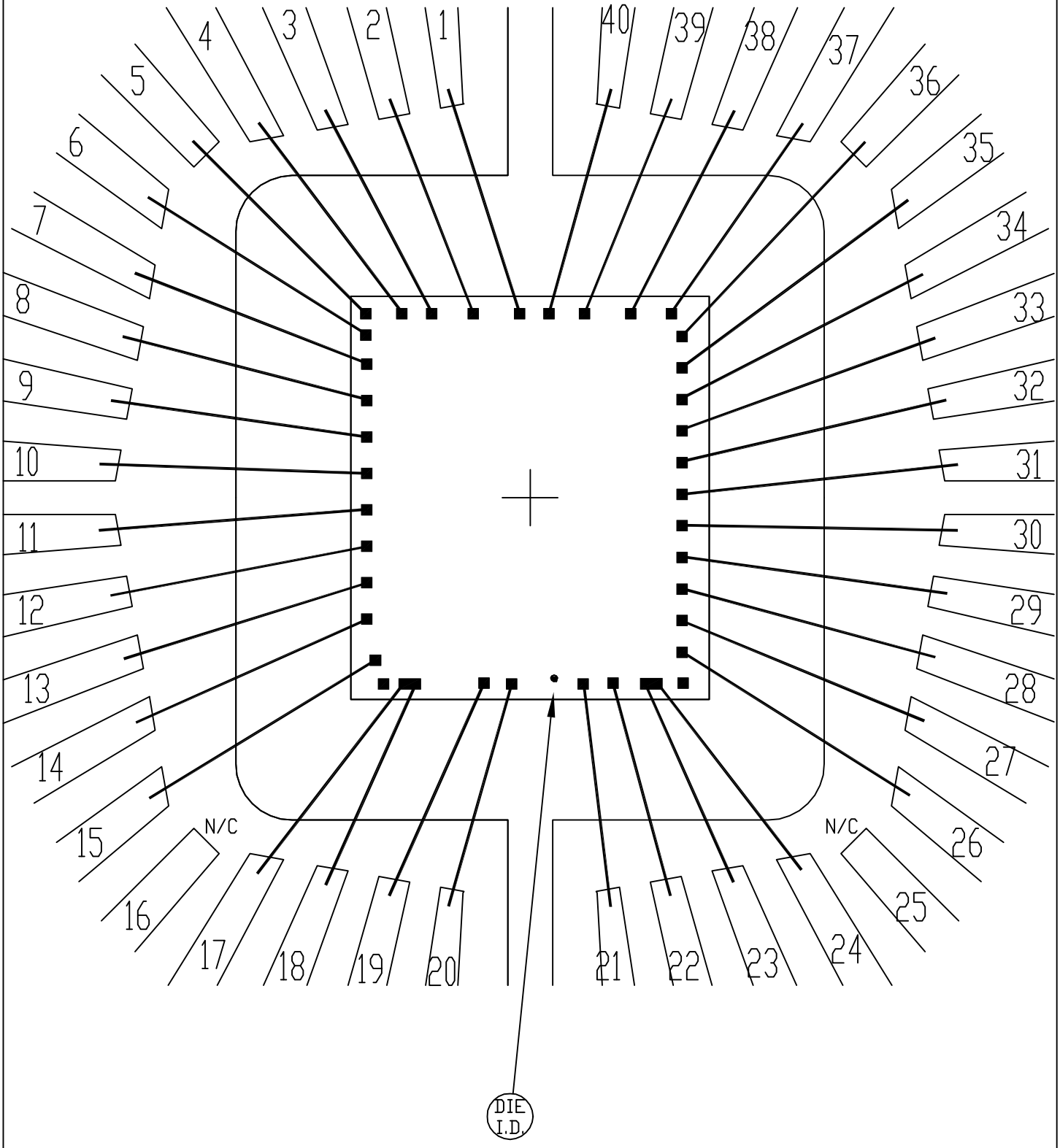
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

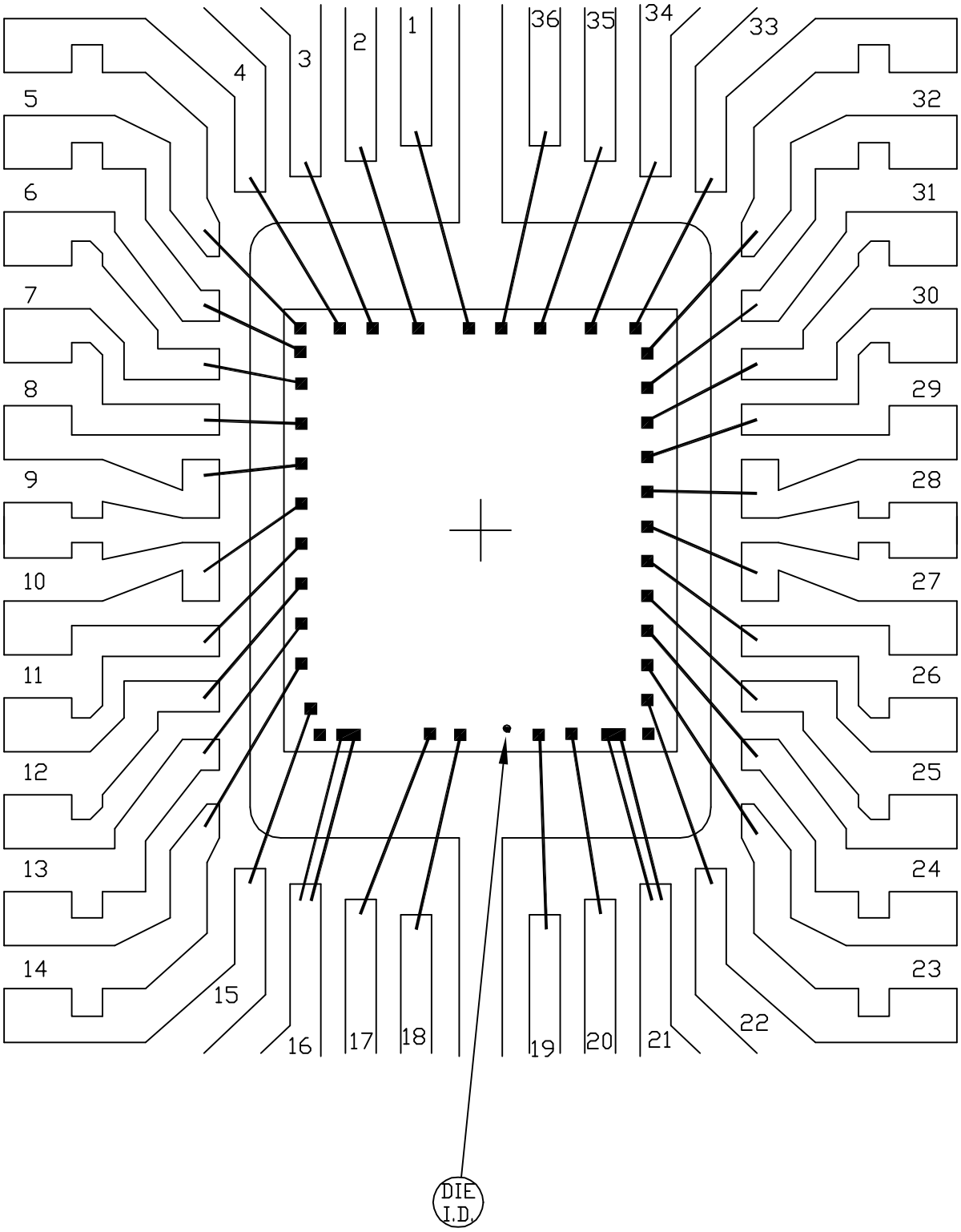
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



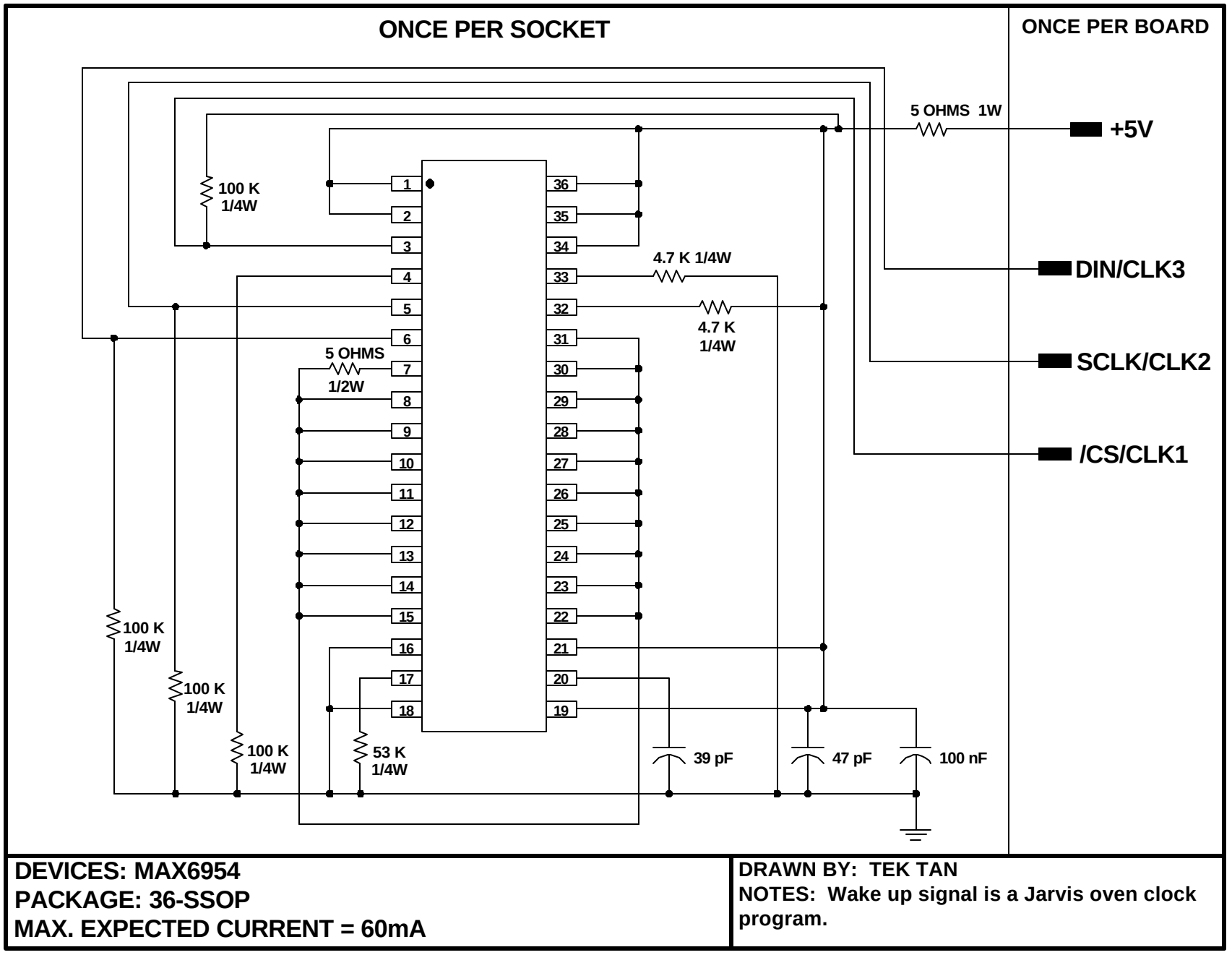

Mil Std 883D
Method 3015.7
Notice 8




| PKG. CODE: P40-2 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 210 X 230 | PKG. | | | BOND DIAGRAM #: 05-3301-0027 | REV: A |
| | DESIGN | | | | |




| | | | | |
|---|---|---|---|---|
| PKG. CODE: A36-2 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY |
| CAV./PAD SIZE: 150X200 | PKG. | | | BOND DIAGRAM #: 05-3301-0026 REV: A |
| | DESIGN | | | |




**DEVICES: MAX6954**
**PACKAGE: 36-SSOP**
**MAX. EXPECTED CURRENT = 60mA**

**DRAWN BY: TEK TAN**
**NOTES: Wake up signal is a Jarvis oven clock program.**