



RELIABILITY REPORT  
FOR  
MAX6960ATH+  
PLASTIC ENCAPSULATED DEVICES

October 14, 2010

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

<b>Approved by</b>
Don Lipps
Quality Assurance
Manager, Reliability Engineering

## Conclusion

The MAX6960ATH+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX6960-MAX6963 are compact cathode-row display drivers that interface microprocessors to 8 x 8 dot-matrix red, green, and yellow (R,G,Y) LED displays through a high-speed 4-wire serial interface. The MAX6960-MAX6963 drive two monochrome 8 x 8 matrix displays, or a single RGY 8 x 8 matrix display with no external components. The driver can also be used with external pass transistors to control red, green, blue (RGB) and other displays at higher currents and voltages. The MAX6960-MAX6963 feature open- and short-circuit LED detection, and provide both analog and digital tile segment current calibration to allow 8 x 8 displays from different batches to be compensated or color matched. A local 3-wire bus synchronizes multiple interconnected MAX6960-MAX6963s and automatically allocates memory map addresses to suit the user's display-panel architecture. The MAX6960-MAX6963s' 4-wire interface connects multiple drivers, with display memory mapping shared and allocated among the drivers. A single global write operation can send a command to all MAX6960s in a panel. The MAX6963 drives monochrome displays with two-step intensity control. The MAX6962 drives monochrome displays with two-step or four-step intensity control. The MAX6961 drives monochrome or RGY displays with two-step intensity control. The MAX6960 drives monochrome or RGY displays with two-step or four-step intensity control.

**II. Manufacturing Information**

A. Description/Function:	4-Wire Serially Interfaced 8 x 8 Matrix Graphic LED Drivers
B. Process:	S4
C. Number of Device Transistors:	120632
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	July 23, 2005

**III. Packaging Information**

A. Package Type:	44-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1003
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	37°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1°C/W

**IV. Die Information**

A. Dimensions:	168 X 143 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$\lambda = 22.9$  F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (ESD lot SJDODQ001C D/C 0640, Latchup lot SJD0CZ003B D/C 0523)

The DW06 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX6960ATH+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SJD0DQ001C, DC 0640

Note 1: Life Test Data may represent plastic DIP qualification lots.