

RELIABILITY REPORT
FOR
MAX6969AxG
PLASTIC ENCAPSULATED DEVICES

April 12, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX6969 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

The MAX6969 serial-interfaced LED driver provides 16 open-drain, constant-current-sinking LED driver outputs rated at 5.5V. The MAX6969 operates from a 3V to 5.5V supply. The MAX6969 supply and the LEDs' supply or supplies can power up in any order. The constant-current outputs are programmed together to up to 55mA using a single external resistor. The MAX6969 operates with a 25Mb, industry-standard, 4-wire serial interface.

The MAX6969 uses the industry-standard, shift-register-plus-latch-type serial interface. The driver accepts data shifted into a 16-bit shift register using data input DIN and clock input CLK. Input data appears at the DOUT output 16 clock cycles later to allow cascading of multiple MAX6969s. The latch-enable input, LE, loads the 16 bits of shift register data into a 16-bit output latch to set which LEDs are on and which are off. The output enable, OE-bar, gates all 16 outputs on and off, and is fast enough to be used as a PWM input for LED intensity control.

For applications requiring LED fault detection, refer to the MAX6984*, which automatically detects open-circuit LEDs.

For safety-related applications requiring a watchdog timer, refer to the MAX6979, which includes a fail-safe feature that blanks the display if the serial interface becomes inactive for more than 1s.

The MAX6969 is one of a family of 12 shift-register-plus-latch-type LED drivers. The family includes 8-port and 16-port types, with 5.5V- or 36V-rated LED outputs, with and without open-circuit LED detection and watchdog. All versions operate from a 3V to 5.5V supply, and are specified over the -40°C to +125°C temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltage with respect to GND.	
V+	-0.3V to +6V
OUT_	-0.3V to +6V
DIN, CLK, LE, OE, SET	-0.3V to (V+ + 0.3V)
DOUT Current	±10mA
OUT_ Sink Current	60mA
Total GND Current	480mA
Continuous Power Dissipation (TA = +70°C)	
24-Pin TSSOP (derate 12.2mW/°C over +70°C)	975mW
24-Pin PDIP (derate 13.3mW/°C over +70°C)	1067mW
24 Wide SO (derate 11.8mW/°C over +70°C)	941mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	16-Port, 5.5V Constant-Current LED Driver
B. Process:	B8/S8
C. Number of Device Transistors:	3858
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	April, 2005

III. Packaging Information

A. Package Type:	24-Pin TSSOP	24-Pin PDIP	24-Pin Wide SO
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin (all packages)		
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1680	# 05-9000-1681	# 05-2901-2104
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 117 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 22.91 \times 10^{-9}$$

$$\lambda = 22.91 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6461) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT Rate of 0.27 @ 25C and 4.64 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DW86 die type has been found to have all pins able to withstand a transient pulse of +/-2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6969AxG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	WSO	77	0
			TSSOP	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

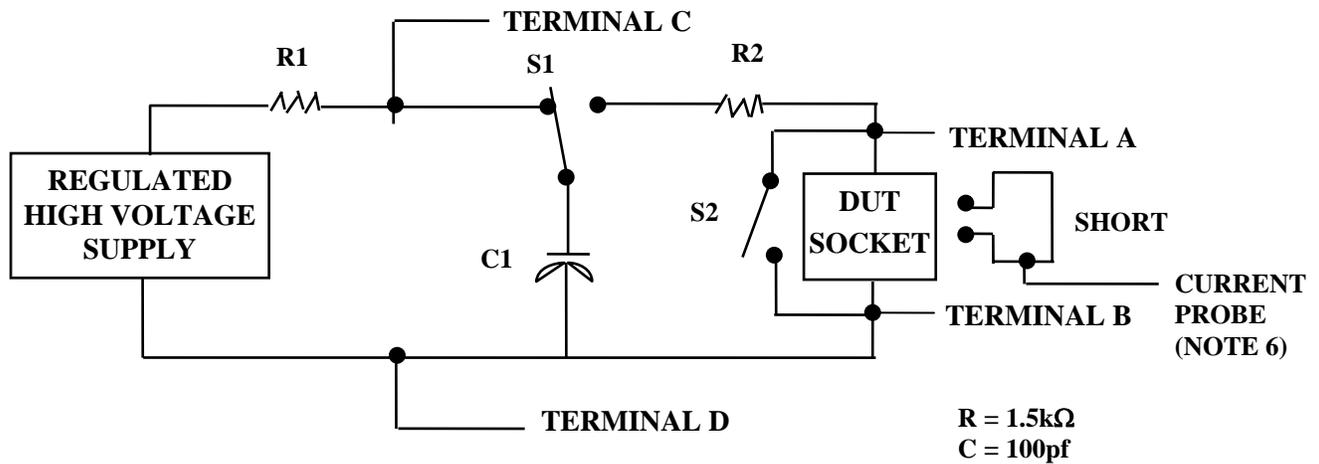
1/ Table II is restated in narrative form in 3.4 below.

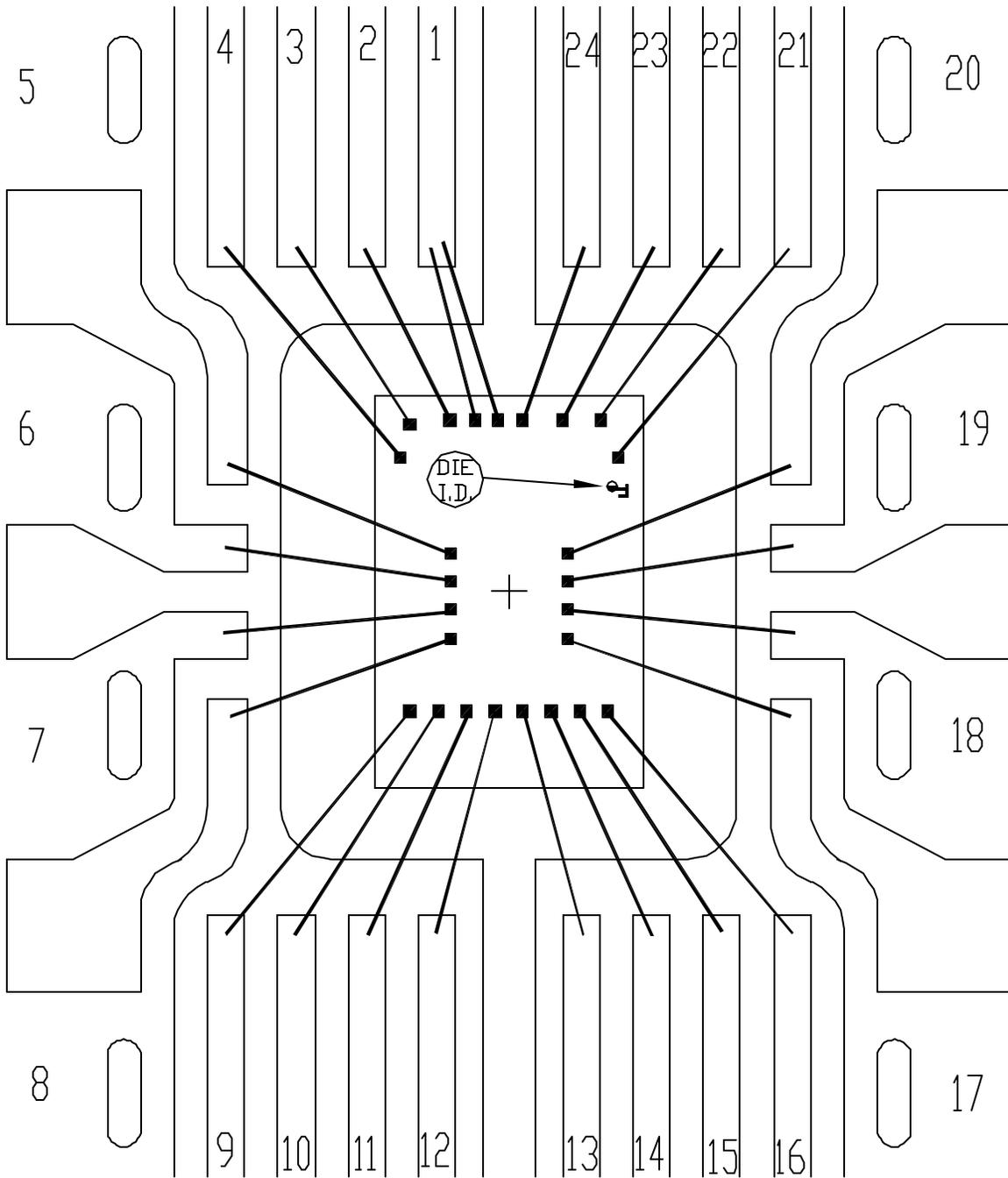
2/ No connects are not to be tested.

3/ Repeat pin combination 1 for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE:
N24-1

SIGNATURES

DATE

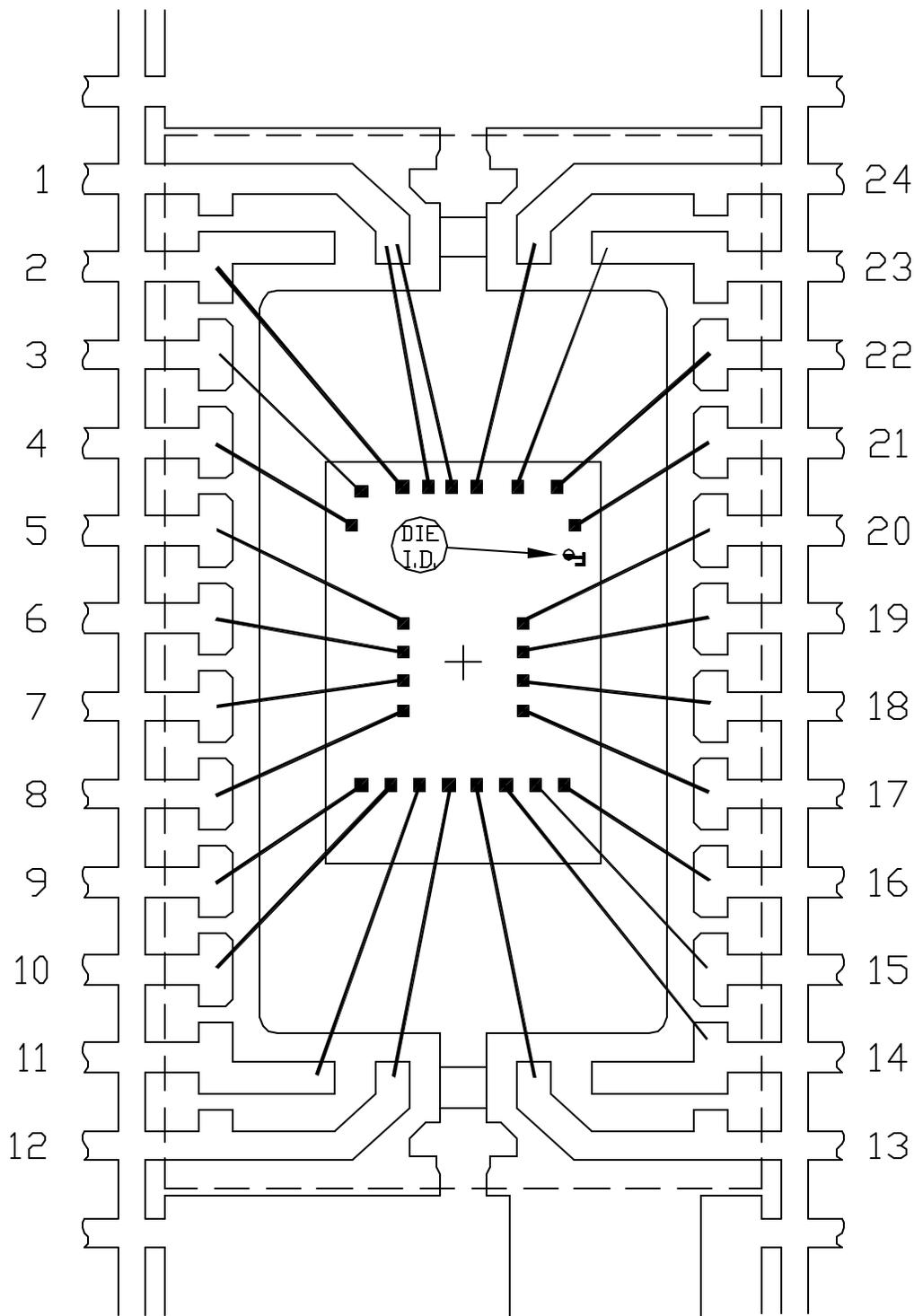
MAXIM
CONFIDENTIAL & PROPRIETARY

CAV./PAD SIZE:
136 X 160

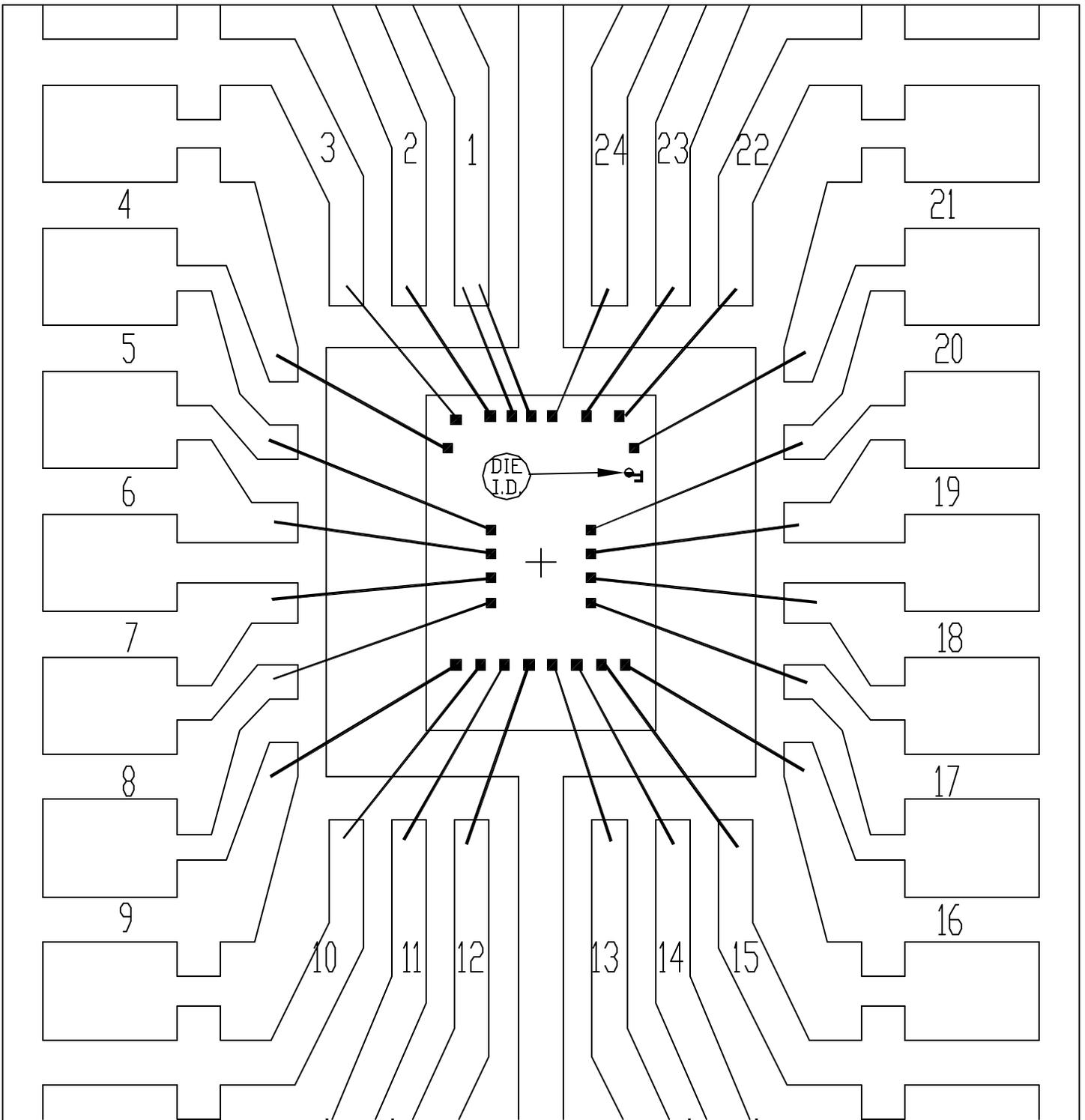
PKG.
DESIGN

BOND DIAGRAM #:
05-9000-1681

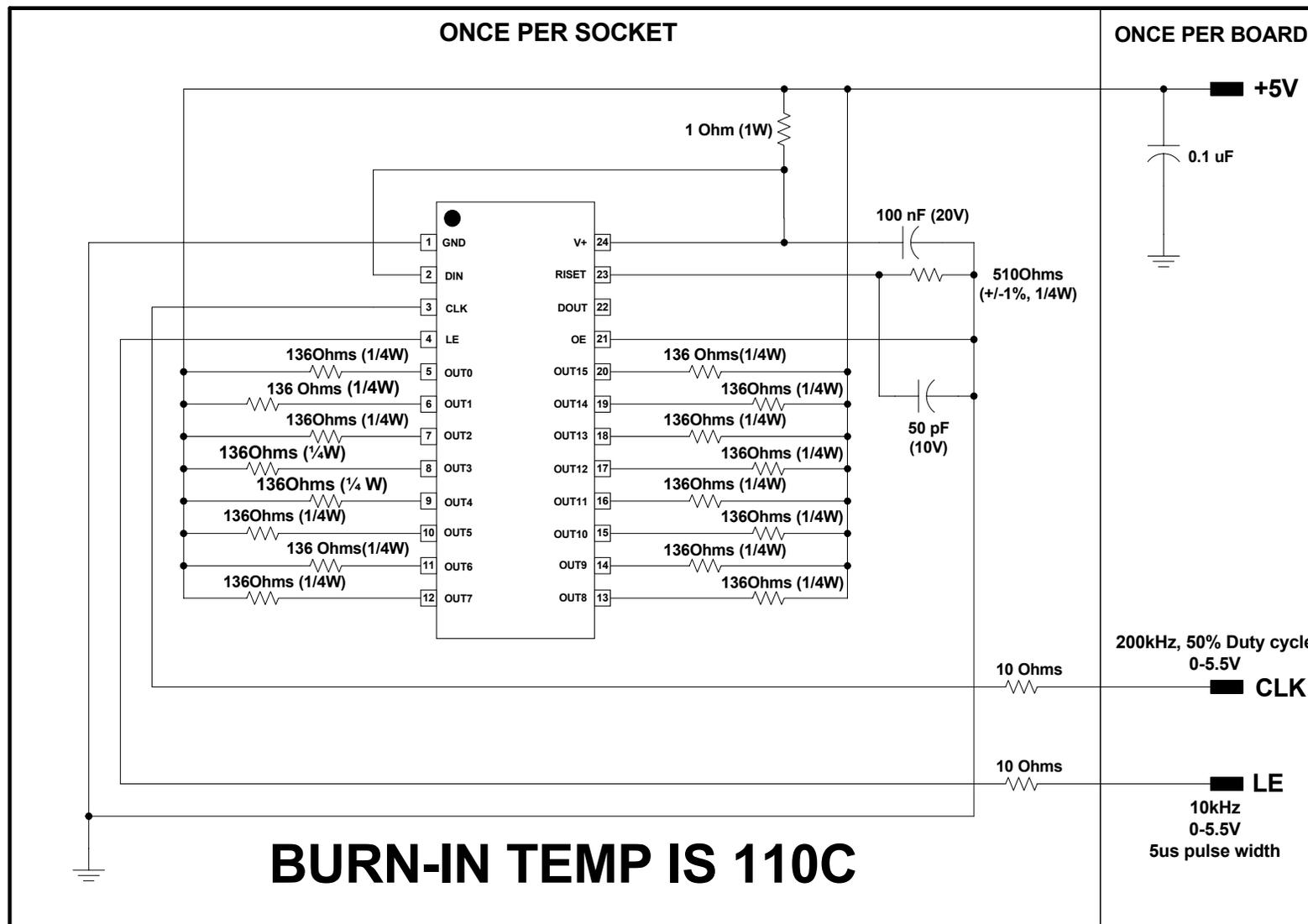
REV:
A



PKG. CODE: U24-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x217	PKG. DESIGN			BOND DIAGRAM #: 05-9000-1680	REV: A



PKG. CODE: W24-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150 X 150	PKG. DESIGN			BOND DIAGRAM #: 05-9000-2104	REV: A



DEVICES: MAX6971AUG-1 (DW87Z)
PACKAGE: 24-TSSOP
MAX. EXPECTED CURRENT = 620mA

NOTES: THE JUNCTION TEMP WILL RISE
ABOUT 35C DURING BURN-IN