RELIABILITY REPORT

FOR

MAX7034AUI+T

PLASTIC ENCAPSULATED DEVICES

January 22, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX7034AUI+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX7034 fully integrated low-power CMOS super-heterodyne receiver is ideal for receiving amplitude-shift-keyed (ASK) data in the 300MHz to 450MHz frequency range (including the popular 315MHz and 433.92MHz frequencies). The receiver has an RF sensitivity of -114dBm. With few external components and a low-current power-down mode, it is ideal for cost-sensitive and power-sensitive applications typical in the automotive and consumer markets. The MAX7034 consists of a low-noise amplifier (LNA), a fully differential image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO), a 10.7MHz IF limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data-recovery circuitry. The MAX7034 is available in a 28-pin (9.7mm x 4.4mm) TSSOP package and is specified over the automotive (-40°C to +125°C) temperature range.

II. Manufacturing Information

A. Description/Function:	315MHz/434MHz ASK Superheterodyne Receiver
B. Process:	0.35um CMOS
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines and Thailand
F. Date of Initial Production:	January 25, 2008

III. Packaging Information

A. Package Type:	28-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2935
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	78°C/W
K. Single Layer Theta Jc:	13°C/W
L. Multi Layer Theta Ja:	71.6°C/W
M. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	78 X 58 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.5 micron (as drawn)
F. Minimum Metal Spacing:	0.45 micron (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{500 \times 4340 \times 143 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.0 \times 10^{-9}$

$\lambda = 3.0$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.8 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QINZAQ003D, D/C 0804)

The LF33 die type has been found to have all pins able to withstand a transient pulse of

ESD-HBM:	+/- 500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX7034AUI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	95	0	QINZAQ003D, D/C 0804
	Biased	& functionality	48	0	QINZAQ002B, D/C 0803
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.