RELIABILITY REPORT

FOR

MAX7311AAG+

PLASTIC ENCAPSULATED DEVICES

November 13, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX7311AAG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX7311 2-wire-interfaced expander provides 16-bit parallel input/output (I/O) port expansion for SMBus(tm) and I²C applications. The MAX7311 consists of input port registers, output port registers, polarity inversion registers, configuration registers, a bus timeout register, and an I²C-compatible serial interface logic compatible with SMBus. The system master can invert the MAX7311 input data by writing to the active-high polarity inversion register. The system master can enable or disable bus timeout by writing to the bus timeout register. Any of the 16 I/O ports can be configured as an input or output. A power-on reset (POR) initializes the 16 I/Os as inputs. Three address select pins configure one of 64 slave ID addresses. The MAX7311 supports hot insertion. All port pins, the active-low INT output, SDA, SCL and the slave address inputs AD0-2 remain high impedance in power down (V+ = 0V) with up to 6V asserted upon them. The MAX7311 is available in 24-pin SO, SSOP, TSSOP, and thin QFN packages and is specified over the -40℃ to +125℃ automotive temperature range. For applications requiring I/Os without pullup resistors, refer to the MAX7312 data sheet.

II. Manufacturing Information

A. Description/Function:	2-Wire-Interfaced 16-Bit I/O Port Expander with Interrupt and Hot-Insertion Protection
B. Process:	C6
C. Number of Device Transistors:	12994
D. Fabrication Location:	California
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	January 25, 2003

III. Packaging Information

A. Package Type:	24-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0116
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	125°C/W
K. Single Layer Theta Jc:	26°C/W
L. Multi Layer Theta Ja:	67°C/W
M. Multi Layer Theta Jc:	25°C/W

IV. Die Information

A. Dimensions:	85X91 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 93 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.8 \times 10^{-9}$

λ = 11.8 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.17 @ 25C and 2.89 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot ILM0EQ001A, D/C 0441)

The DW53 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX7311AAG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	SLM2EY003A, D/C 0516
	Biased	& functionality	45	0	ILM0BQ001A, D/C 0245
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.