RELIABILITY REPORT

FOR

MAX732CWE+T

PLASTIC ENCAPSULATED DEVICES

December 6, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX732CWE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX732/MAX733 are CMOS step-up DC-DC switch-mode regulators. The MAX732 is a +12V regulator that accepts inputs from 4.0V to 9.3V and delivers up to 200mA of DC current. The MAX733 is a +15V regulator that delivers up to 125mA and accepts inputs from 4.0V to 11.0V. Typical full-load efficiencies are 85% to 92%. They require only a single inductor value of 50uH to function over their entire ranges, so no inductor -related design is necessary. Accuracy is guaranteed over temperature, line, and load variations. The MAX732/MAX733 use a current-mode pulse-width modulation (PWM) controller to provide precise output regulation and low subharmonic noise. Typical no load supply current is 1.7mA. Fixed 170kHz oscillator frequencies allow easy filtering of ripple and noise and provide for small external components. The MAX732/MAX733 feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection. For an adjustable version of these devices, refer to the MAX752 data sheet. For lower-power step-up applications, refer to the MAX632/MAX633 and MAX642/MAX643 data sheets. For more applications information, refer to AN-41, MAX732 EV Surface-Mount Evaluation Board and Flash EEPROM Power Supply Application Notes.

II. Manufacturing Information

A. Description/Function:	+12V/+15V Step-Up Current-Mode PWM Regulators
B. Process:	SG5
C. Fabrication Location:	USA
D. Assembly Location:	Philippines, Malaysia
E. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	16-pin SOIC (W)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0701-0594
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	105°C/W
K. Single Layer Theta Jc:	22°C/W
L. Multi Layer Theta Ja:	70°C/W
M. Multi Layer Theta Jc:	23°C/W

IV. Die Information

A. Dimensions:	114X123 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 640 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.72 \times 10^{-9}$

$\lambda = 1.72$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PS63 die type has been found to have all pins able to withstand an HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX732CWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	640	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.