

RELIABILITY REPORT
FOR
MAX792xxxE
PLASTIC ENCAPSULATED DEVICES

March 3, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX792 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX792 microprocessor (μ P) supervisory circuit provides the most functions for power-supply and watchdog monitoring in systems without battery backup. Built-in features include the following:

- 1) μ P reset: Assertion of RESET and /RESET outputs during power-up, power-down, and brownout conditions. /RESET is guaranteed valid for V_{CC} down to 1V.
- 2) Manual-reset input.
- 3) Two-stage power-fail warning: A separate low-line comparator compares V_{CC} to a preset threshold 120mV above the reset threshold; the low-line and reset thresholds can be programmed externally.
- 4) Watchdog fault output: Assertion of /WDO if the watch-dog input is not toggled within a preset timeout period.
- 5) Pulsed watchdog output: Advance warning of impending /WDO assertion from watchdog timeout that causes hardware shutdown.
- 6) Write protection of CMOS RAM, EEPROM, or other memory devices.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Input Voltage (with respect to GND)	
V_{CC}	-0.3V to +6V
All Other Inputs	-0.3V to ($V_{CC} + 0.3V$)
Input Current	
GND	25mA
All Other Outputs	25mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
16-Pin SO	696mW
16-Pin DIP	842mW
Derates above +70°C	
16-Pin SO	9.52mW/°C
16-Pin DIP	10.53mW/°C

II. Manufacturing Information

A. Description/Function:	Microprocessor and Non-Volatile Memory Supervisory Circuit
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	950
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	October, 1993

III. Packaging Information

A. Package Type:	16-Lead NSO	16-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0701-0658	# 05-0701-0657
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1	Level 1

IV. Die Information

A. Dimensions:	70 x 78 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability, Operation Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 480 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 2.26 \times 10^{-9} \quad \lambda = 2.26 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0039) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PS95 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 50\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX792xxxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		480	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

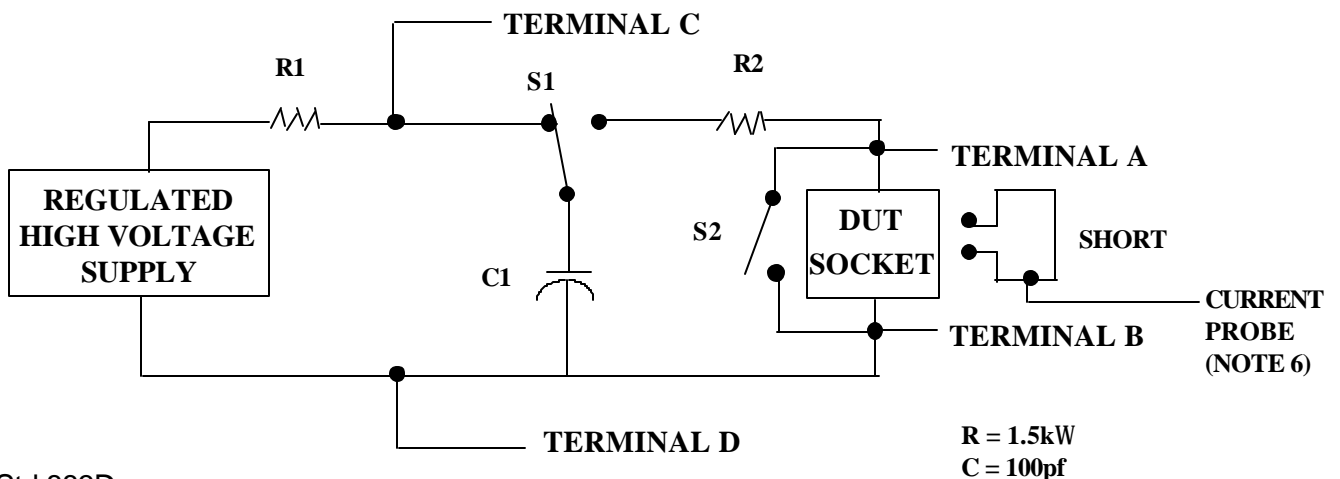
2/ No connects are not to be tested.

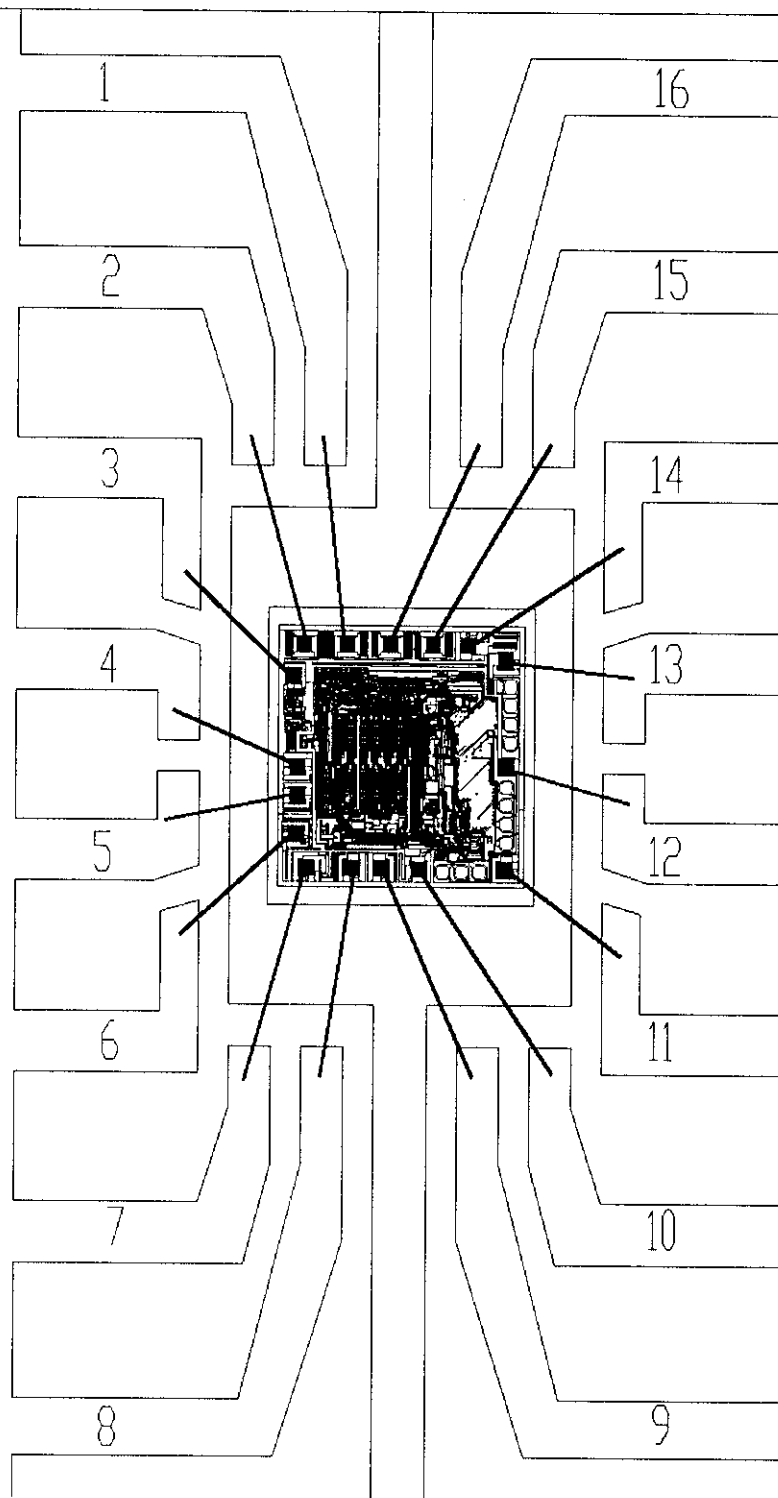
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG CODE: S16-2

CAV./PAD SIZE: 90 X 130

APPROVALS

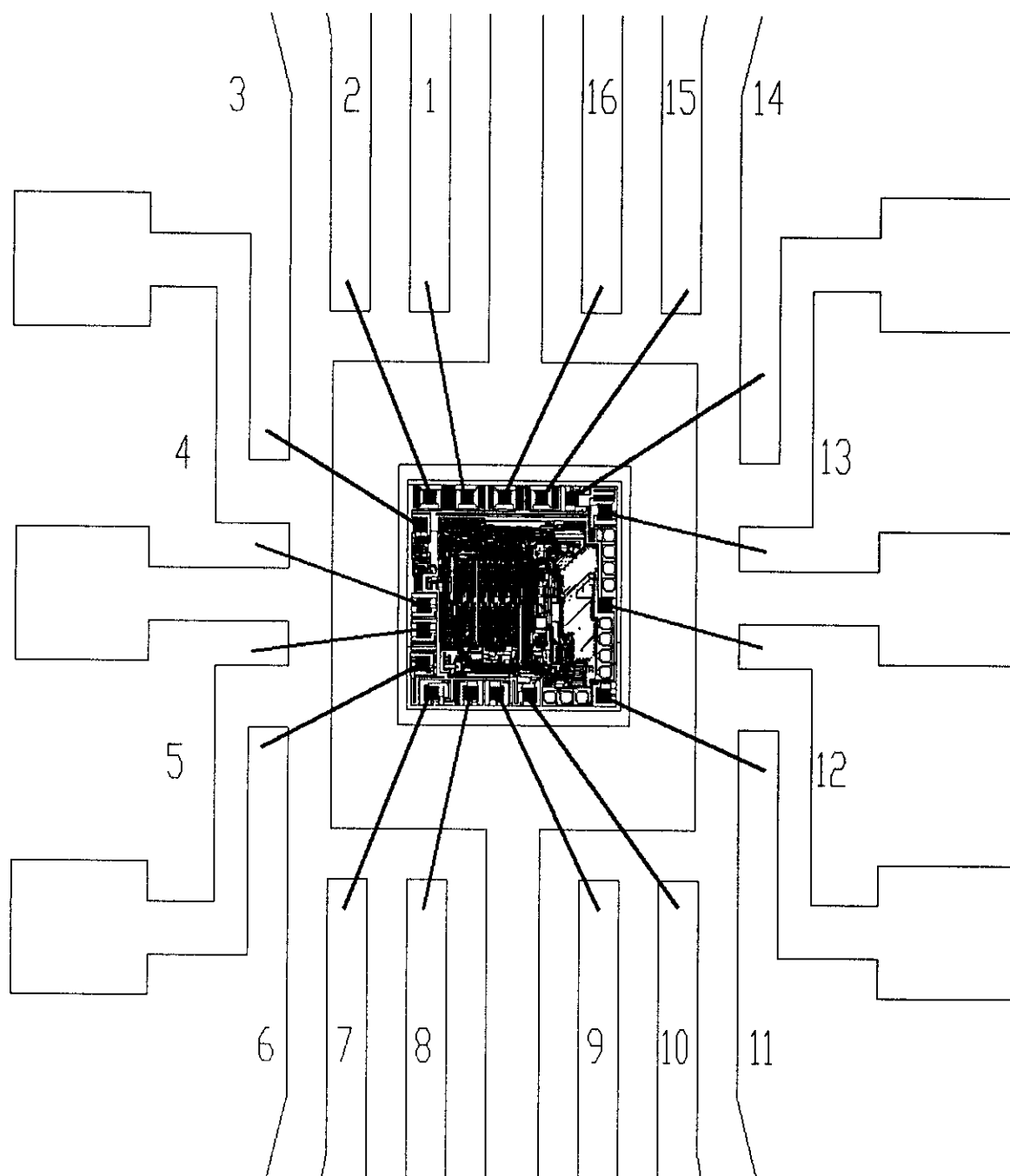
DATE

MAXIM

BUILDSHEET NUMBER:
05-0701-0658

REV:
A

PKG.
DESIGN



PKG.CODE: P16-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-0701-0657
				REV: A

